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A REDUCED-SWITCH THREE-LEVEL FIVE-PHASE INVERTER WITH SVM-BASED COMMON-MODE VOLTAGE ELIMINATION AND CURRENT HARMONIC SUPPRESSION FOR OPEN-END WINDING DRIVES

Huu-Cong Vu[1], **Duc-Khanh Hoang**[2], **Quoc-Hoan Tran**[3*]

[1]*Hanoi University of Civil Engineering Hanoi, Vietnam*

[2]*Institute of Energy, Ministry of Industry and Trade Hanoi, Vietnam*

[3]*Tran Dai Nghia University Ho Chi Minh City, Vietnam*

*Email: *hoantq@tdnu.edu.vn*

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ABSTRACT

Although the dual five-phase voltage source inverter (VSI) was previously developed to extend output voltage levels in five-phase open-end winding drives without requiring clamping diodes or DC-link capacitor balancing, its active switch count remains equivalent to that of the three-level five-phase neutral-point-clamped topology at 20 devices. This paper addresses that limitation by introducing a novel reduced-switch three-level five-phase VSI that employs only 15 active switches, achieving a 25% reduction in device count. Complementing the hardware contribution, a tailored space vector modulation (SVM) scheme is formulated to achieve complete common-mode voltage elimination and suppression of low-order current harmonics. The validity of the proposed inverter and its SVM strategy is confirmed through simulation studies.

Keywords: Reduced-switch five-phase voltage source inverter, common-mode voltage elimination, current harmonic suppression, open-end winding drives, space vector modulation.

1. INTRODUCTION

Multiphase drive technology and five-phase systems in particular have gained growing attention within the research community owing to the inherent performance benefits they provide relative to standard three-phase architectures. Key benefits include distributed power handling across phases, superior torque ripple characteristics, higher torque-per-ampere capability, additional degrees of freedom for independent flux and torque regulation, and robustness under open-circuit fault conditions [1]-[3]. These properties collectively establish five-phase drives as a preferred candidate for demanding applications, including naval electric propulsion, traction in electric and hybrid vehicles, aerospace actuators, and offshore wind generation systems [3]-[6].

Power converters for five-phase drives are typically realized through either two-level topologies or multilevel configurations, the most prevalent of which is the neutral-point-clamped (NPC) inverter [7]. Transitioning from two-level to three-level operation brings measurable improvements: the synthesized output voltages exhibit lower harmonic content, the demands on passive output filtering are relaxed, the inverter thermal stress is better distributed, and electromagnetic interference generated by high dv/dt switching events is mitigated [8].

Despite these benefits, the three-level five-phase NPC inverter is not without fundamental shortcomings. On the hardware side, the classical NPC structure demands a substantial number of clamping diodes alongside the primary switching devices, translating into increased bill-of-materials cost, greater physical volume, and additional thermal management challenges, all of which degrade achievable power density. On the control side, the requirement to actively regulate the voltage balance across the split DC-link capacitors introduces considerable algorithmic overhead that complicates implementation and diminishes practical viability in medium- and high-power contexts.

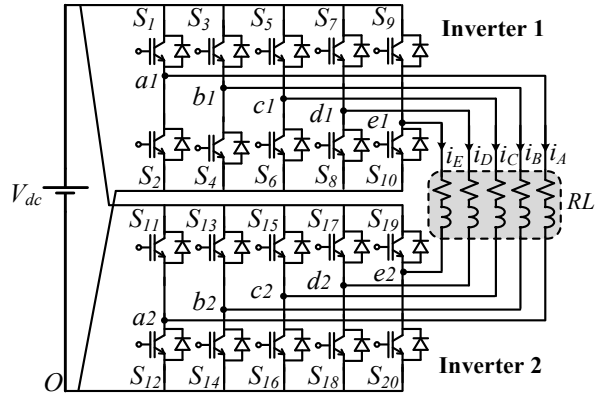

Fig. 1. The dual five-phase voltage source inverter (DFVSI) topology [10]

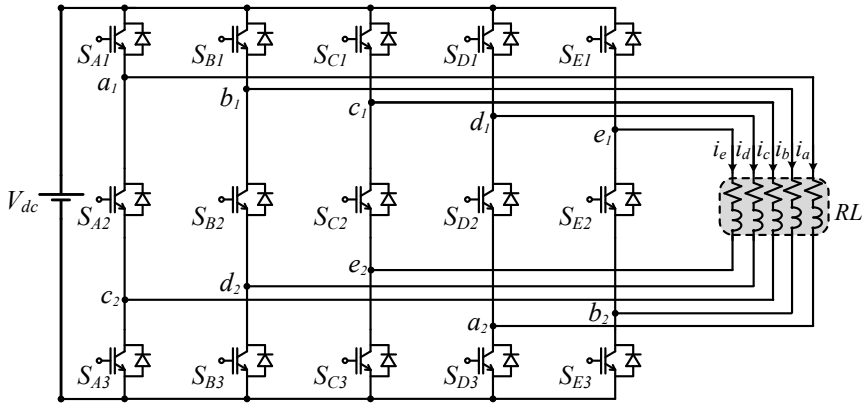

Fig. 2. The proposed reduced switch three-level five-phase VSI

The T-type converter family was explored in [9] as a means of reducing the device count inherent in NPC structures, and it does achieve a meaningful reduction in the number of active switches. However, this approach does not resolve the fundamental capacitor voltage imbalance problem, since the split DC-link architecture is preserved; consequently, the associated control burden persists. A more complete solution to the balancing issue was proposed in [10] through the dual five-phase voltage source inverter (DFVSI) concept shown in Fig. 1, which dispenses with both clamping diodes and split DC-link capacitors entirely. Nevertheless, realizing a complete five-phase drive with this architecture still necessitates 20 active switching devices - a figure on par with the conventional NPC inverter - leaving hardware cost, switching losses, and integration complexity at unacceptably high levels.

The foregoing discussion reveals a clear design gap: no existing three-level five-phase topology simultaneously achieves a low switch count and freedom from DC-link capacitor

balancing requirements. Motivated by this observation, this work introduces the inverter topology depicted in Fig. 2, which is designed to satisfy both criteria concurrently.

The introduced topology conveys two distinct contributions over the existing art. With respect to hardware, the active switch count is trimmed from 20 to 15 - a 25% reduction - directly lowering component procurement cost and enabling a more compact power stage footprint. With respect to control, by avoiding a split DC-link, the topology is inherently immune to capacitor voltage imbalance, eliminating an entire layer of supervisory control logic and improving the dependability of the overall system. Together, these attributes render the topology attractive for cost-sensitive, space-constrained, high-reliability five-phase drive platforms such as traction inverters, shipboard propulsion drives, and industrial servo systems.

While the hardware architecture constitutes a necessary prerequisite for high performance, the quality of the drive output is ultimately governed by the modulation algorithm. In open-end winding five-phase systems supplied by a single DC bus, inappropriate vector selection can excite CMV and inject low-order harmonic currents through the $(x-y)$ subspace, both of which are detrimental to efficiency and waveform quality. Accordingly, this paper develops a purpose-built SVM algorithm for the 15-switch topology with two co-equal design objectives: complete elimination of CMV across all operating conditions, and nullification of $(x-y)$ subspace voltage components to suppress the associated low-order current harmonics.

2. PROPOSED REDUCED-SWITCH THREE-LEVEL FIVE-PHASE VSI TOPOLOGY

2.1. Circuit Structure

The power circuit of the proposed inverter, shown in Fig. 2, comprises five three-switch legs - one per phase - all connected to a single DC source of voltage V_{dc}. Each terminal of the open-end winding load is tied to the corresponding upper and lower output nodes of its respective inverter leg, granting the topology the flexibility to impose bipolar phase voltages. Within each leg, two mandatory switching constraints govern device operation: all three switches may not conduct simultaneously, since this would create a destructive shoot-through path across the DC bus; and no fewer than two switches may be active at any given instant, ensuring that a continuous freewheeling path is maintained for load current.

Under these constraints, each inverter leg is restricted to three valid switching states, as listed in Table 1. As a result, the proposed five-phase 15-switch inverter can generate three distinct voltage levels at the output of each phase. Accordingly, the phase voltage $V_x\left(x=a,b,c,d,e\right)$ of the inverter can be expressed by the following equation:

$$V_x = V_{mO} - V_{nO} \tag{1}$$

where $V_{mO}\left(m=a_1,b_1,c_1,d_1,e_1\right)$ and $V_{nO}\left(n=a_2,b_2,c_2,d_2,e_2\right)$ represent the pole voltages of the upper and lower output terminals of each inverter leg, respectively.

Table 1. Switching states of each leg of the proposed topology.

Switching State	S_{X1} $(X=A,B,C,D,E)$	S_{X2} $(X=A,B,C,D,E)$	S_{X3} $(X=A,B,C,D,E)$	V_{mO} $(m=a_1,b_1,c_1,d_1,e_1)$	V_{nO} $(n=a_2,b_2,c_2,d_2,e_2)$
2	1	1	0	V_{dc}	V_{dc}
1	1	0	1	V_{dc}	0
0	0	1	1	0	0

The five-phase fifteen-switch inverter can generate 243 distinct switching state combinations, each corresponding to a unique voltage vector. By applying the vector space decomposition (VSD) transformation matrix [11], these voltage vectors are mapped into the $(\alpha-\beta)$ and $(x-y)$ subspaces, as given by:

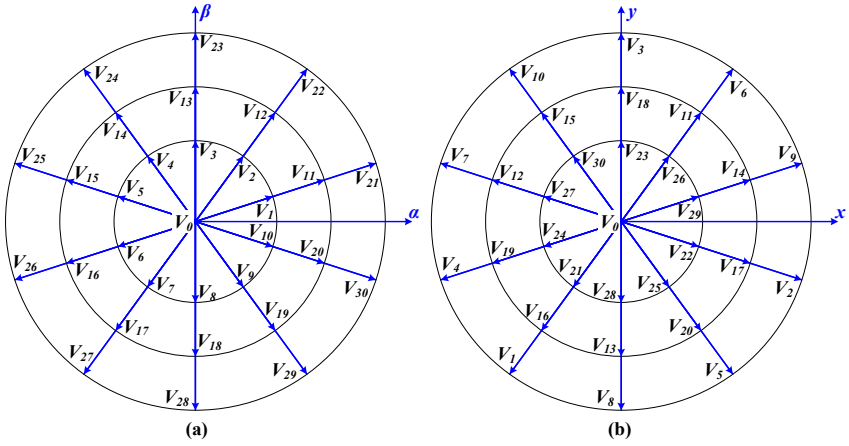

Fig. 3. Voltage vector spaces with zero CMV of the proposed topology: (a) $(\alpha-\beta)$ space, and (b) $(x-y)$ space

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_x \\ V_y \end{bmatrix} = \frac{2}{5}\begin{bmatrix} 1 & \cos\delta & \cos 2\delta & \cos 3\delta & \cos 4\delta \\ 0 & \sin\delta & \sin 2\delta & \sin 3\delta & \sin 4\delta \\ 1 & \cos 3\delta & \cos\delta & \cos 4\delta & \cos 2\delta \\ 0 & \sin 3\delta & \sin\delta & \sin 4\delta & \sin 2\delta \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix} \tag{2}$$

where $\delta = 2\pi/5$.

Through the vector space decomposition (VSD) transformation, output voltage harmonic components of order $m = 10k \pm 1\ (k = 0,1,2,...)$ are mapped into the $(\alpha-\beta)$ space, whereas harmonic components of order $m = 10k \pm 3\ (k = 0,1,2,...)$ are projected onto the $(x-y)$ space. The voltage components appearing in the $(x-y)$ subspace generate low-order current harmonics with relatively large amplitudes. Therefore, effective suppression of these components is crucial for improving the output current quality [6], [11].

2.2. Comparison

Table 2 benchmarks the proposed topology against three representative three-level five-phase VSI configurations from the literature, using four hardware metrics: active switch count, clamping diode count, DC-link capacitor count, and the number of isolated DC supplies required. Across all configurations surveyed, the proposed design achieves the lowest active device count and is the only topology that requires neither clamping diodes nor DC-link capacitors, while being compatible with a single, non-isolated DC supply. This combination results in the most streamlined power stage and the least demanding control implementation among the alternatives compared.

Table 2. Comparative evaluation of the proposed topology and conventional three-level five-phase VSI configurations

Topology	Number of active switches	Number of capacitors	Number of diodes	Number of DC sources
Topology [8]	20	2	10	1
Topology [9]	20	7	0	1
Topology [10]	20	0	0	1
The proposed topology	15	0	0	1

2.3. Common-Mode Voltage

The common-mode voltage (CMV) of the proposed three-level five-phase inverter can be expressed as follows [6]:

$$V_{CMV} = \frac{\left(V_A + V_B + V_C + V_D + V_E\right)}{5} \tag{3}$$

Because the proposed inverter operates from a single, non-isolated DC supply, the load neutral is referenced to the DC bus, and any non-zero CMV will drive common-mode current through parasitic paths. The resulting common-mode current introduces additional conduction losses, elevates bearing current stress in motor loads, and corrupts the output current waveforms. Accordingly, CMV elimination is not merely a desirable objective but a fundamental requirement for maintaining acceptable efficiency and output current quality [6].

3. SVM-BASED CMV ELIMINATION FOR THE PROPOSED TOPOLOGY

From the preceding analysis, it is clear that two distinct phenomena limit output quality in the proposed five-phase 15-switch drive: CMV-induced common-mode current, which raises losses and compromises electromagnetic compatibility; and active voltage projections onto the $(x-y)$ subspace, which manifest as prominent low-order harmonic currents in the load. A modulation strategy that independently tolerates either phenomenon would be insufficient; both must be simultaneously addressed. This dual suppression requirement forms the central design constraint imposed on the proposed SVM algorithm.

Evaluating (3) across all 243 switching combinations reveals that 31 vectors produce identically zero CMV; their distribution across the two-dimensional subspaces is depicted in Fig. 3. These zero-CMV vectors populate ten evenly spaced sectors and fall naturally into four groups differentiated by their magnitude in the $(\alpha-\beta)$ plane, as detailed in Table 3. Of particular importance are groups L_3 and L_4, which contain the largest $(\alpha-\beta)$ magnitudes yet carry opposite $(x-y)$ components for vectors sharing the same spatial orientation - illustrated by the pairing of V_{11} and V_{21}. This geometrical duality provides a direct mechanism: a weighted combination of one L_3 vector and one L_4 vector can be found that yields a nonzero $(\alpha-\beta)$ component while driving the $(x-y)$ contribution to zero. Leveraging this property, all 20 vectors from groups L_3 and L_4, augmented by the zero vector from group L_1, are used to synthesize 11 virtual voltage vectors that form the basis of the proposed SVM strategy.

Table 3. Amplitude of the voltage vectors with zero CMV

Group	Voltage vector	$\lvert V_{\alpha\beta}\rvert$	$\lvert V_{xy}\rvert$	V_{CMV}
L_1	V_0	0	0	0
L_2	$V_1 - V_{10}$	$0.47023V_{dc}$	$0.76085V_{dc}$	0
L_3	$V_{11} - V_{20}$	$0.76085V_{dc}$	$0.47023V_{dc}$	0
L_4	$V_{21} - V_{30}$	$1.23107V_{dc}$	$0.29062V_{dc}$	0

3.1. Virtual Voltage Vector Synthesis

The complete set of 11 virtual vectors is partitioned into two functional groups: group I contains a single null vector V_Z, while group II encompasses the ten active virtual vectors. The virtual zero voltage vector V_Z is constructed from the original zero voltage vector V_0 and can be expressed as:

$$\begin{cases} V_z = 0 \\ V_{z\alpha\beta} = V_{0\alpha\beta} = 0 \\ V_{zxy} = V_{0xy} = 0 \end{cases} \tag{4}$$

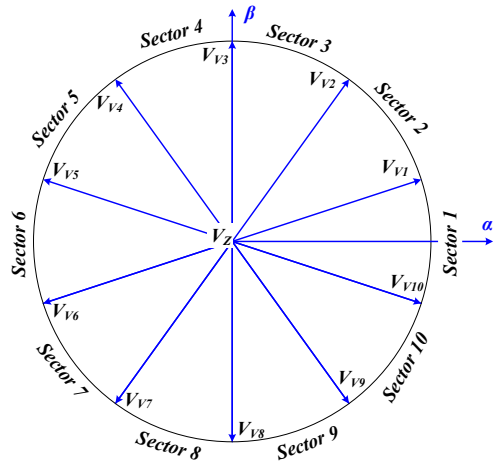

Fig. 4. Distribution of the virtual voltage vectors in the $(\alpha - \beta)$ space for the proposed SVM

Each virtual voltage vector in group II is constructed by combining one voltage vector selected from group L_3 with another selected from group L_4. For example, a given virtual voltage vector V_{V1} is synthesized using a voltage vector V_{11} from group L_3 and its corresponding voltage vector V_{21} from group L_4. This relationship can be expressed as follows:

$$\begin{cases} V_{V1\alpha\beta} = d_1 V_{11\alpha\beta} + d_2 V_{21\alpha\beta} \\ V_{V1xy} = d_1 V_{11xy} + d_2 V_{21xy} \end{cases} \tag{5}$$

The coefficients d_1 and d_2 are determined subject to the following constraints:

$$\begin{cases} V_{V1xy} = d_1 V_{11xy} + d_2 V_{21xy} = 0 \\ d_1 + d_2 = 1 \end{cases} \tag{6}$$

From (6), the coefficients d_1 and d_2 are obtained as follows:

$$\begin{cases} d_1 = 0.382 \\ d_2 = 0.618 \end{cases} \tag{7}$$

By substituting the values of d_1 and d_2 into (5), the virtual voltage vector in the $(\alpha-\beta)$ and $(x-y)$ subspaces can be obtained as follows:

$$\begin{cases} V_{V1\alpha\beta} = d_1 V_{11\alpha\beta} + d_2 V_{21\alpha\beta} = 1.0514 V_{dc} \angle 18^\circ \\ V_{V1xy} = d_1 V_{11xy} + d_2 V_{21xy} = 0 \end{cases} \tag{8}$$

Table 4. Magnitudes of the proposed virtual voltage vectors

Group	Voltage vector	$\lvert V_{\alpha\beta}\rvert$	$\lvert V_{xy}\rvert$	V_{CMV}
I	V_Z	*0*	*0*	*0*
II	$V_{V1} - V_{V10}$	$1.0514V_{dc}$	*0*	*0*

Similarly, the remaining virtual voltage vectors are constructed following the same principle, as illustrated in Fig. 4. As summarized in Table 4, all 11 virtual voltage vectors exhibit zero voltage components in the $(x-y)$ space, while the CMV is eliminated.

3.2. Proposed SVM Method

The voltage vector diagram of the proposed SVM method is divided into ten distinct sectors. Specifically, sector 1 spans the angular range from $-\pi/10$ to $\pi/10$, while each subsequent sector is obtained by rotating the previous one counterclockwise by an angle of $\pi/5$, as illustrated in Fig. 4.

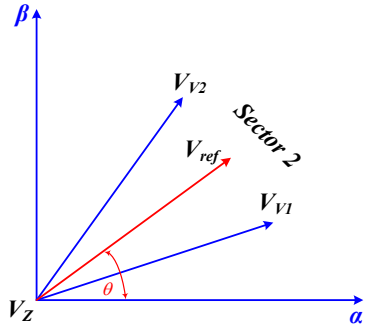

Fig. 5. Reference output voltage vector synthesis in the proposed SVM method

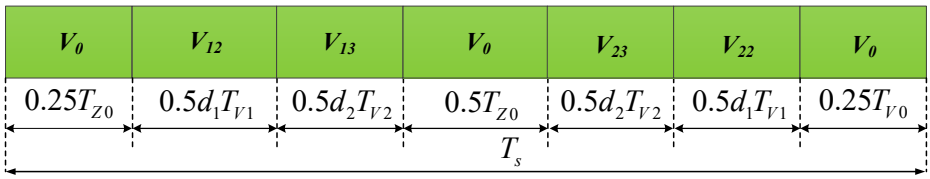

Fig. 6. Switching sequence of the proposed SVM method in sector 2

The synthesis of the reference output voltage vector is achieved by combining the three nearest virtual voltage vectors. For example, when the reference voltage vector is located in sector 2, as illustrated in Fig. 5, the virtual voltage vectors V_z, V_{V1} and V_{V2} are selected to synthesize the desired output voltage vector. The corresponding dwelling times are then determined according to the following constraints:

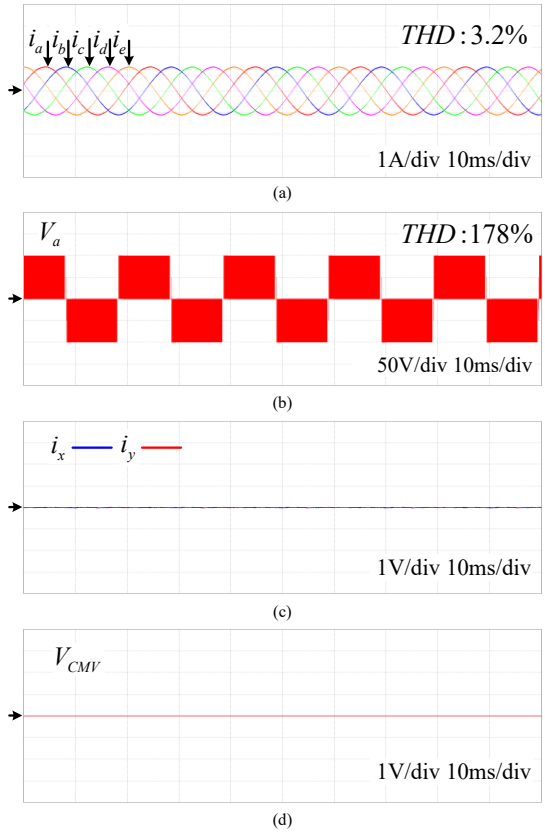

Fig. 7. Simulation results of the proposed SVM method at m_a=*0.3*: (a) output current i_a, i_b, i_c, i_d, i_e; (b) output phase voltage V_a; (c) output current in (*x -y)* space; and (d) CMV

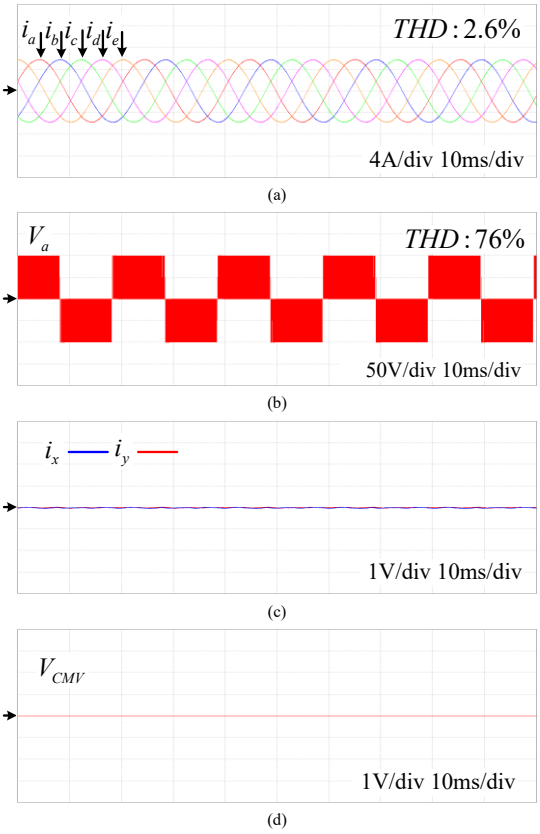

Fig. 8. Simulation results of the proposed SVM method at m_a=*0.8*: (a) output current i_a, i_b, i_c, i_d, i_e; (b) output phase voltage V_a; (c) output current in (*x -y)* space; and (d) CMV

$$\begin{cases} T_s V_{ref} = T_{Z0} V_Z + T_{V1} V_{V1} + T_{V2} V_{V2} \\ T_s = T_{Z0} + T_{V1} + T_{V2} \end{cases} \tag{9}$$

where T_{Z0}, T_{V1} and T_{V2} denote the duration times associated with the virtual voltage vectors V_Z, V_{V1} and V_{V2}, respectively. In addition, T_s represents the sampling period.

Consequently, the corresponding duration times can be obtained as follows:

$$\begin{cases} T_{V1} = -1.61813 m_a \sin\left(\dfrac{19\pi}{10} - \theta\right) \\ T_{V2} = -1.61813 m_a \sin\left(\theta - \dfrac{\pi}{10}\right) \\ T_{Z0} = 1 - T_{V1} - T_{V2} \end{cases} \tag{10}$$

where $m_a = V_{ref} / V_{dc}$ is the modulation index.

Once the three optimal virtual voltage vectors and their corresponding dwell times are determined, an appropriate switching sequence is generated and applied to control the inverter. Fig. 6 illustrates the resulting switching sequence for the case in which the reference voltage vector is located in sector 2.

By employing these virtual voltage vectors, the proposed SVM method effectively eliminates the CMV and significantly reduces low-order current harmonics. However, the proposed SVM method inherently results in a reduced maximum modulation index. This reduction reflects a trade-off between voltage utilization capability and improved output performance, including CMV elimination and harmonic suppression.

4. SIMULATION RESULTS

The proposed inverter and the proposed SVM method are assessed by time-domain simulation in PSIM under the following conditions: $V_{dc} = 100V$; five-phase R-L load ($R = 13\Omega$, $L = 15mH$); fundamental output frequency of 50 Hz; sampling period $T_s = 100\mu s$.

Performance is examined at two modulation indices representative of light-load (m_a = *0.3*) and near-rated (m_a = *0.8*) operation. At m_a = *0.3*, Fig. 7 presents the five-phase load currents, phase voltage, $(x-y)$ current trajectory, and CMV waveform. The load currents, shown in Fig. 7(a), are well-balanced and quasi-sinusoidal with a measured THD of 3.2%, confirming good current quality despite the relatively low modulation index. The phase voltage in Fig. 7(b) exhibits the expected three-level staircase profile with a voltage THD of 178%, consistent with operation at a low modulation index. Critically, Figs. 7(c) and 7(d) demonstrate that both the $(x-y)$ current components and the CMV are driven to negligible levels, providing direct empirical validation of the dual-suppression objectives of the proposed SVM method.

Increasing the modulation index to m_a = *0.8* (Fig. 8) allows the performance of the proposed inverter ceiling to be assessed. The CMV trace in Fig. 8(d) remains identically zero across the entire waveform, and the $(x-y)$ current locus in Fig. 8(c) collapses to the origin, confirming that the SVM method maintains its dual-suppression properties independent of operating point. Furthermore, the higher modulation index utilizes the available DC-link more efficiently, reducing the phase current THD from 3.2% to 2.6% and compressing the phase voltage THD from 178% to 76%.

Table 5. Comparison of power losses and efficiency between the conventional DFVSI and the proposed inverter

Parameter	Conventional DFVSI	Proposed Inverter
Conduction loss (W)	35.7	57.8
Switching loss (W)	4.6	3.4
Total loss (W)	40.3	61.2
Efficiency (%)	96.8%	95.1%

A comprehensive comparison of power losses and efficiency between the proposed inverter and the conventional DFVSI [10] has been conducted using PSIM simulations, as summarized in Table 5. The evaluation is performed based on the IGBT device model IXGH40N60C2 600V/40 A. The loss calculation is derived from the datasheet parameters of the manufacturer, including conduction characteristics and switching energy curves (E_{on}, E_{off}), ensuring that the simulated results closely reflect practical device behavior. The results demonstrate that the proposed inverter exhibits lower switching losses, mainly due to the reduced number of active switches. However, its conduction losses are higher, which can be attributed to the altered current conduction paths in the 15-switch configuration, where more devices may participate in the current path under certain operating states. As a result, the overall power loss of the proposed inverter is slightly higher, leading to a marginal reduction in efficiency (95.1%)

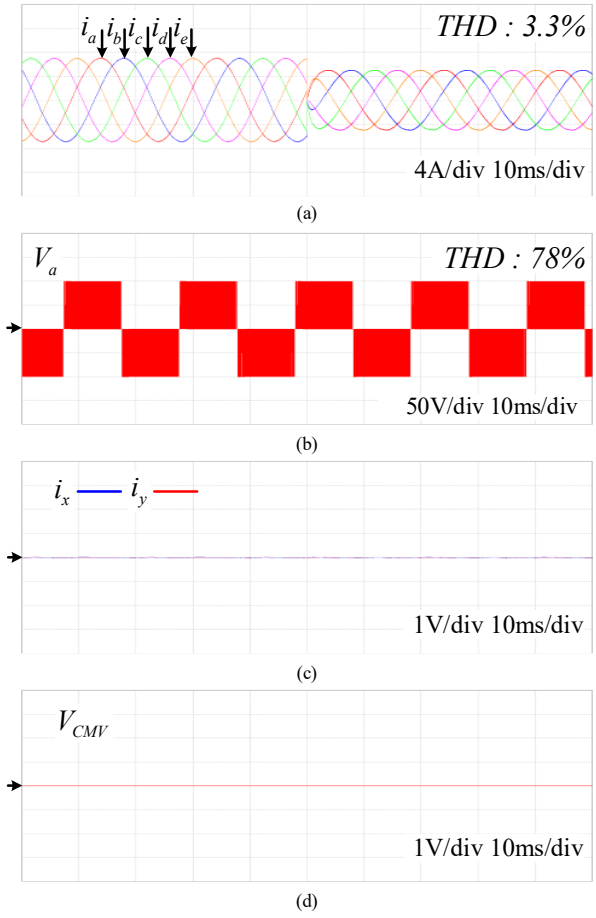

Fig. 9. Dynamic performance of the proposed inverter under R-L load variation

compared to the conventional topology (96.8%). The efficiency reduction remains relatively small and acceptable when considering the significant advantages of the proposed inverter. Therefore, the proposed inverter should not be regarded as a direct replacement aiming to outperform existing solutions in all aspects, but rather as a practical approach that provides an effective balance between efficiency, system complexity, and cost.

To further assess the dynamic performance of the proposed inverter, a load step-change test was conducted in the simulation. Specifically, the R-L load parameters were varied during operation: from 0 to 0.2 s, the load is set to $R = 10\,\Omega$ and $L = 15$ mH, and from 0.2s onward, the load is changed to $R = 15\,\Omega$ and $L = 10$mH. Fig. 9 shows that the phase currents remain nearly sinusoidal with low harmonics (THD = 3.3%) despite the abrupt load variation. The output phase voltage preserves the expected multilevel characteristics, while the CMV is effectively suppressed. In addition, the currents in the $(x-y)$ space remain close to zero, suggesting that the associated harmonic components are well mitigated. These findings confirm that the proposed inverter as well as the proposed SVM method exhibit strong robustness against load disturbances, ensuring stable operation and high-quality output waveforms under dynamic conditions.

5. CONCLUSION

This paper has presented a reduced switch three-level five-phase VSI for open-end winding loads, addressing the inherent limitations of conventional five-phase inverters,

particularly NPC and DFVSI configurations. By employing only 15 active power switches, the proposed inverter significantly reduces the semiconductor device count while maintaining the capability to generate multilevel output voltages for five-phase open-end loads. In addition to the hardware simplification, an SVM method has been proposed. Through the appropriate selection and synthesis of 11 virtual voltage vectors, the proposed SVM method completely eliminates the CMV and effectively suppresses low-order current harmonics, thereby improving the overall output current quality and system performance. Simulation results have verified the effectiveness and feasibility of both the proposed inverter and the proposed SVM method. Owing to the reduced number of switching devices, effective elimination of CMV, and enhanced output current quality, the proposed solution demonstrates strong potential for medium- and high-power five-phase drive applications, particularly in systems requiring a compact structure, high reliability, and cost-effective implementation.

REFERENCES

[1] A. Bhowate, M. V. Aware, and S. Sharma, "Predictive torque control algorithm for a five-phase induction motor drive for reduced torque ripple with switching frequency control," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7282–7294, Jul. 2020, doi: https://doi.org/10.1109/TPEL.2019.2954991.

[2] H. -C. Vu and H. -H. Lee, "Simple MPCC Strategy for Three-Level Sparse Five-Phase VSI to Suppress Current Harmonics With Balanced Neutral-Point Voltage," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 771-781, Jan. 2022, doi: https://doi.org/10.1109/TPEL.2021.3094193.

[3] H. Vu and H. Lee, "Common-Mode Voltage and Current Harmonic Reduction for Five-Phase VSIs with Model Predictive Current Control," Journal of Power Electronics, vol. 19, no. 6, pp. 1477–1485, Nov. 2019, doi: https://doi.org/10.6113/JPE.2019.19.6.1477.

[4] U. R. Muduli, B. Chikondra and R. K. Behera, "Space Vector PWM Based DTC Scheme With Reduced Common Mode Voltage for Five-Phase Induction Motor Drive," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 114-124, Jan. 2022, doi: https://doi.org/10.1109/TPEL.2021.3092259.

[5] M. Medina-Sánchez, A. G. Yepes, Ó. López and J. Doval-Gandoy, "Assessment and Exploitation of the Minimum Current Harmonic Distortion Under Overmodulation in Five-Phase Induction Motor Drives," *IEEE Transactions on Power Electronics*, vol. 38, no. 4, pp. 4289-4305, April 2023, doi: https://doi.org/10.1109/TPEL.2022.3231138.

[6] H. C. Vu and H. H. Lee, "Simplified model predictive current control strategy for dual five-phase VSI-fed open-end load to eliminate common-mode voltage and reduce current harmonics," *Journal of Power Electronics*, vol. 21, no. 8, pp. 1155–1165, Aug. 2021, doi: https://doi.org/10.1007/s43236-021-00266-0.

[7] S. Payami, R. K. Behera, A. Iqbal and R. Al-Ammari, "Common-Mode Voltage and Vibration Mitigation of a Five-Phase Three-Level NPC Inverter-Fed Induction Motor Drive System," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 349-361, June 2015, doi: https://doi.org/10.1109/JESTPE.2014.2313153.

[8] S. Payami, R. K. Behera and A. Iqbal, "DTC of Three-Level NPC Inverter Fed Five-Phase Induction Motor Drive With Novel Neutral Point Voltage Balancing Scheme," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1487-1500, Feb. 2018, doi: https://doi.org/10.1109/TPEL.2017.2675621.

[9] A. A. Gandomi, S. Saeidabadi and L. Parsa, "A Fault Tolerant T-type Inverter for Five-phase PMSM Drives," *IECON 2019 - 45th Annual Conference of the IEEE Industrial*

Electronics Society, Lisbon, Portugal, 2019, pp. 834-839, doi: https://doi.org/10.1109/IECON.2019.8927164.

[10] N. Bodo, M. Jones and E. Levi, "A Space Vector PWM With Common-Mode Voltage Elimination for Open-End Winding Five-Phase Drives With a Single DC Supply," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2197-2207, May 2014, doi: https://doi.org/10.1109/TIE.2013.2272273.

[11] Q. -H. Tran and H. -H. Lee, "An Advanced Modulation Strategy for Three-to-Five-Phase Indirect Matrix Converters to Reduce Common-Mode Voltage With Enhanced Output Performance," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5282-5291, July 2018, doi: https://doi.org/10.1109/TIE.2017.2782242.