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ANALYSIS OF HEAT LOSS AND OPEN CIRCUIT FAULT ON T-NPC INVERTER IN WIND ENERGY CONVERSION SYSTEM

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ABSTRACT

This research provides an in-depth analysis of thermal losses and open-circuit fault tolerance of the three-level T-Type Neutral Point Clamped (T-NPC) inverter, applied in the power conversion system of a wind energy conversion system. The core objective is to evaluate the thermal performance and reliability of the T-NPC topology compared to the conventional Neutral Point Clamped (NPC) structure, which is particularly crucial in high-reliability wind power systems. The paper conducts a comparative study on both the three-level NPC and T-NPC inverter topologies under the same Carrier-Based Pulse Width Modulation (CPWM) strategy. The research delves into the analysis of conduction losses and switching losses for individual IGBT and diodes. The thermal analysis results reveal a significant difference in total thermal losses across the components. Due to the specific topology and the duty cycle distribution inherent in CPWM, the T-NPC configuration exhibits a notable uneven thermal distribution across its legs, yet achieves a reduction in total switching losses compared to the NPC under identical operating conditions. The central focus of this study is the investigation of the effects of the open-circuit fault occurring at the T-branch of the T-NPC inverter. Based on the fault impact analysis on the output voltage quality and wind energy conversion system current, the paper proposes a suitable control method based on Carrier-Based PWM. This method enables the system to continue operating with acceptable harmonic quality (Fault-Tolerant Control) upon the detection of an open-circuit fault in the T-branch. These findings and proposals provide crucial data for the selection and design of highly efficient and reliable three-level inverters for renewable energy applications.

Keywords: Inverter voltage source, T bridge inverter, Open circuit error, Total harmonic distortion, PWM technique.

1. INTRODUCTION

The rapid growth of Renewable Energy Sources (RES), particularly wind power systems utilizing wind energy conversion system, has amplified the demand for highly reliable and efficient power electronic converters[1]. wind energy conversion system are favored for their high power density, compact size, and brushless operation. However, integrating wind energy conversion system into the grid or load systems necessitates inverters that can guarantee high-quality AC output. As the power ratings of these wind energy conversion system increase to medium and large scales (ranging from several hundred kW to megawatts), conventional Two-Level Inverters demonstrate significant limitations [2], [3]. These drawbacks include requiring

high voltage-rated power switches, generating large output voltage harmonics, and suffering from high filtering losses. To overcome these constraints, Multilevel Inverters have become the industry standard solution. Multilevel Inverters effectively divide the DC-link voltage into multiple levels, thereby reducing the voltage stress imposed on individual semiconductor switches, allowing for the use of lower voltage-rated devices, significantly improving the Total Harmonic Distortion (THD) of the output voltage, and reducing the filter size. Among the various three-level Multilevel Inverters topologies, the Neutral Point Clamped inverter is the most widely researched and applied structure [4], [5]. Nevertheless, the NPC suffers from drawbacks such as the requirement for numerous clamping diodes and often faces challenges related to DC-link voltage imbalance and non-uniform switching loss distribution. Recently, the Three-Level T-Type NPC inverter has emerged as an attractive alternative. The T-NPC topology eliminates the clamping diodes, replacing them with lower-voltage-rated semiconductor switches in the neutral leg (T-branch), which potentially reduces the overall component count, minimizes volume, and offers the potential for improved efficiency. However, a comprehensive evaluation of the T-NPC topology still presents several critical research gaps. Firstly, although the T-NPC offers structural advantages, a precise and quantified comparison of its thermal performance and total power losses against the standard NPC, particularly under the widely utilized Carrier-Based Pulse Width Modulation strategy, has not been systematically established. The crucial distinction in conduction losses and switching losses between T-NPC and NPC under these specific operating conditions must be thoroughly clarified. Secondly, reliability remains a paramount criterion in wind power applications. Open-circuit faults are the most common failure modes in semiconductor switches. Given the T-NPC's unique structure [6], [7], the T-branch utilizes lower voltage-rated components with distinct thermal and reliability characteristics, making the analysis of open-circuit faults specifically at this branch critically important. Existing Fault-Tolerant Control (FTC) methods often focus on two-level or standard NPC inverters. There is a pressing need for a robust FTC method tailored for the T-NPC topology, leveraging the characteristics of CPWM/FPWM, to ensure continuous operation with maintained acceptable harmonic quality following a T-branch fault.

To address these deficiencies, this research aims to provide the following contributions: Perform a detailed comparative analysis of thermal losses (conduction and switching) between the three-level NPC and [8], Analyze the impact of an open-circuit fault specifically occurring at the T-branch of the T-NPC inverter on the output voltage and current quality, Propose a novel Fault-Tolerant Control method based on CPWM (FPWM) for the T-NPC, enabling the system to sustain continuous operation with acceptable output harmonic quality upon the detection of a T-branch open-circuit fault.

The remainder of this paper is organized as follows: Section II describes the inverter topologies and the applied CPWM strategy [9], [10]. Section III presents the loss calculation model and the thermal performance comparison results. Section IV outlines the open-circuit fault modeling and proposes the FPWM-based FTC method. Finally, concludes the research findings and proposals.

2. DESCRIBES THE INVERTER STRUCTURES AND THE APPLIED CPWM CONTROL METHOD

The comparative study focuses on two crucial three-level voltage source inverter (3L-VSI) topologies. The neutral point clamped and the T-Type Neutral Point Clamped. Both configurations utilize two DC-link capacitors (C_1 and C_2) to generate three distinct voltage levels ($+V_{DC}/2$, 0, $-V_{DC}/2$) at the AC output terminals.

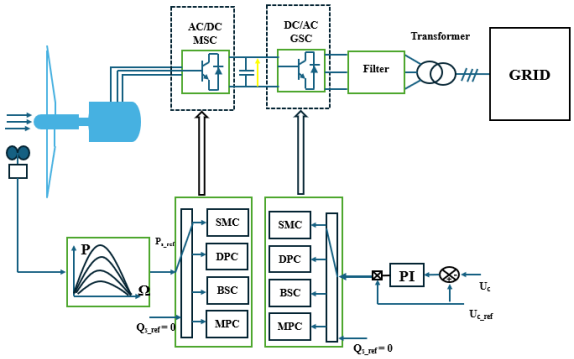


Figure 1. Configuration of a wind energy conversion system

2.1. The neutral point clamp

The neutral point clamp structure uses four active IGBT switches and two clamping diodes for each phase branch. The clamping diodes maintain the neutral point zero voltage and facilitate three output voltage levels. The disadvantage of this structure is that it is susceptible to neutral point voltage fluctuations and inherently has uneven loss distribution between the outer and inner switches (due to unequal conduction times), resulting in asymmetric thermal stress on the phase branch components.

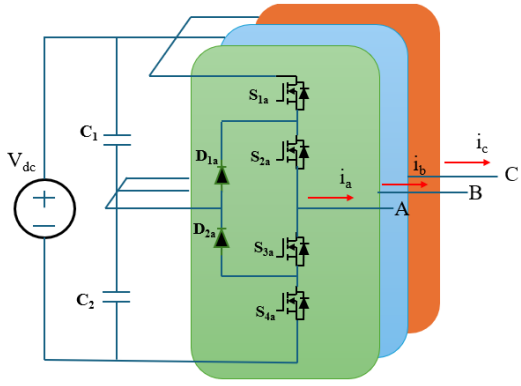


Figure 2. The three-level neutral point clamp

2.2. T-Type Neutral Point Clamped Topology

The 3L-T-NPC uses four active switches for each phase branch, replacing the clamping diodes with two internal switches (S2 and S3), which are typically lower voltage rated devices (e.g., a 600 V switch on a 1200 V DC bus) because they are connected directly to the neutral point.

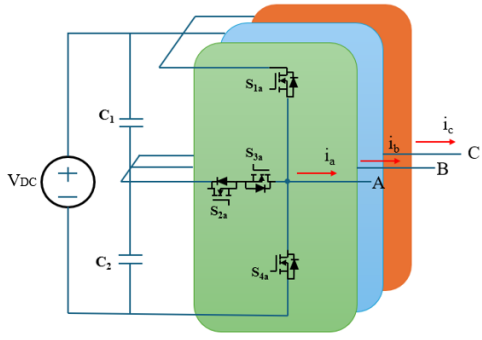


Figure 3. T-Type Neutral Point Clamped

The T-NPC design simplifies the circuit layout and typically provides higher performance under certain operating conditions than the NPC due to fewer components in the main current path.

The two internal switches, forming a T-branch connection to the neutral point, are critical to the switching of the neutral current and are the focus of open circuit fault analysis due to their distinct thermal profiles.

2.3. Carrier-Based PWM Strategy

The Carrier-Based Pulse Width Modulation in Figure 4 strategy is selected for controlling both topologies due to its ease of implementation, computational efficiency, and compatibility with advanced modulation techniques.

CPWM generates the required switching patterns by comparing the three-phase reference voltages (Vref, a}, Vref, b, Vref, c) with two high-frequency triangular carriers (Vcar1 and Vcar2). The compare state transition gives the following voltage levels for phase x (where Vcar1 is the positive carrier and Vcar2 is the negative carrier)

Level P ($V_{DC}/2$): If Vref, x > Vcar1

Level O (0V): If Vcar2 < Vref, x < Vcar1

Level N ($V_{DC}/2$): If Vref, x < Vcar2

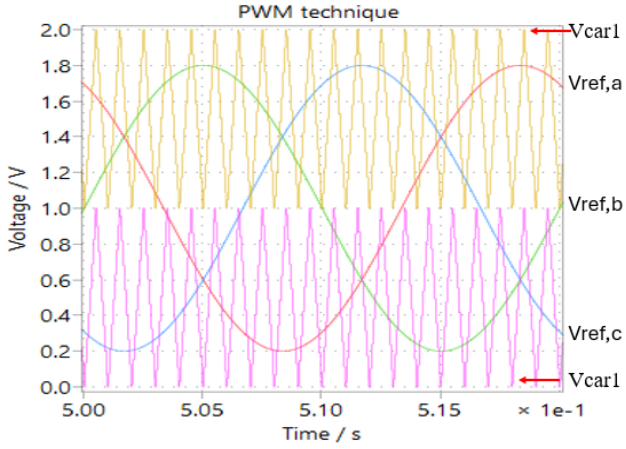


Figure 4. Classical carrier wave modulation technique

To maximize the linear modulation range and achieve the highest possible voltage utilization (equivalent to SVPWM performance), a zero-series voltage bias (typically the introduction of a third-order harmonic component) is added to the sinusoidal reference voltage. This optimized CPWM ensures symmetrical switching patterns and is necessary for a fair temperature comparison between NPC and T-NPC structures. The temperature evaluation analysis on PLECS software will be presented in the next section.

3. PRESENT THE LOSS CALCULATION MODEL AND THERMAL EFFICIENCY COMPARISON RESULTS

3.1. Power Loss Calculation Model (P_{loss})

Accurate analysis of the thermal performance of the NPC and T-NPC topologies is contingent upon establishing a comprehensive power loss model for the semiconductor devices (IGBT and Diode). The total power loss for a phase leg is the sum of conduction losses (P_{cond}) and switching losses (P_{sw}).

Conduction losses are calculated based on the following general device model:

$$P_{cond} = V_T \cdot I_{avg} + R_{on} \cdot {I_{rms}}^2 \quad (1)$$

Where I_{avg} and I_{rms} are the average and RMS current values flowing through the component, respectively. V_T represents the threshold voltage, and R_{on} is the ON-state resistance. The V-I characteristics utilized for calculating the conduction loss of the IGBT 5SNA1600N170100 component are sourced from the PLECS software library.

$$P_{sw} = f_{sw} \frac{1}{T} \int_{0+\phi}^{\frac{T}{2}} (E_{on} + E_{off}) dt \quad (2)$$

Where E_{on} and E_{off} are the energy dissipated during the semiconductor device's turn-on and turn-off switching times, and f_{sw} is the switching frequency. These power loss characteristics of the component are stored in the utility features of the PLECS software.

3.2. Loss analysis using CPWM technique

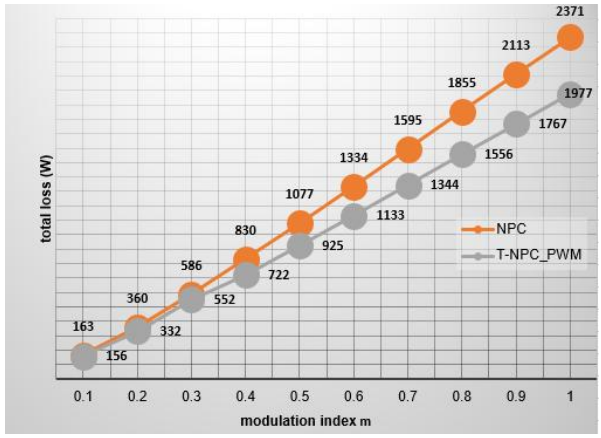


Figure 5. Total losses on the NPC and T-NPC inverters using CPWM technique.

The comparison shown in Figure 5 demonstrates a clear and theoretically expected result: the T-Type NPC inverter exhibits lower total power losses than the conventional NPC inverter across the linear modulation range. This advantage stems primarily from the switching losses. In the T-NPC structure, the inner switches (T-branch) only commute across $V_{DC}/2$. Since P_{sw} is proportional to the square of the voltage during commutation, the reduced voltage stress on these frequently utilized switches dramatically lowers the overall P_{sw}. Therefore, the T-NPC offers a higher overall efficiency and minimizes the requirement for the cooling system. This finding is highly consistent with current literature in power electronics and confirms the validity of the established loss model using component characteristics from databases like PLECS.

4. OUTLINES THE OPEN-CIRCUIT FAULT MODELING AND PROPOSES THE PWM-BASED FTC METHOD

4.1. Open-Circuit Fault (OCF) Modeling in T-NPC Inverters

The non-uniform thermal distribution observed in Section III confirms that the outer switches (S_1, S_4) and the inner T-branch switches (S_2, S_3) of the T-NPC are under different stress levels, increasing the probability of Open-Circuit Fault - the most common fault type in power converters. This section focuses on the OCF occurring in the inner T-branch (e.g., S_{2a} or S_{3a} in phase A in Figure 6) due to its critical role in neutral point current commutation.

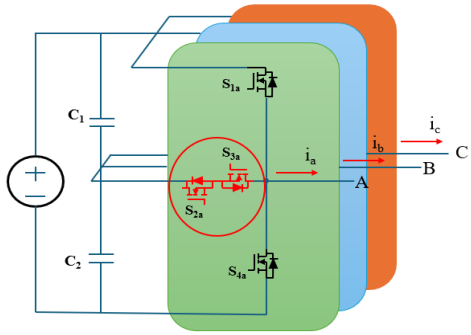
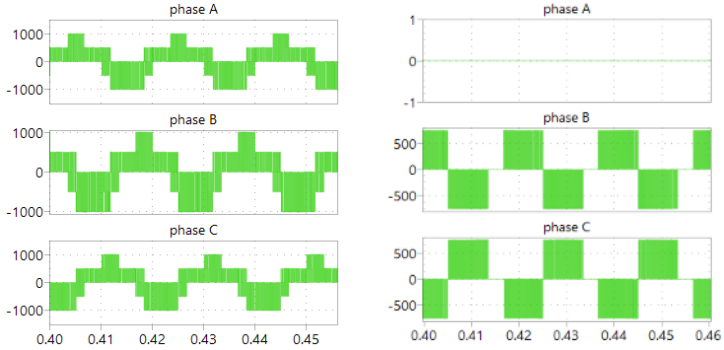


Figure 6. Open circuit fault in branch T on 3-phase T-NPC inverter.

4.2. Impact of Open-Circuit Fault in the inverter

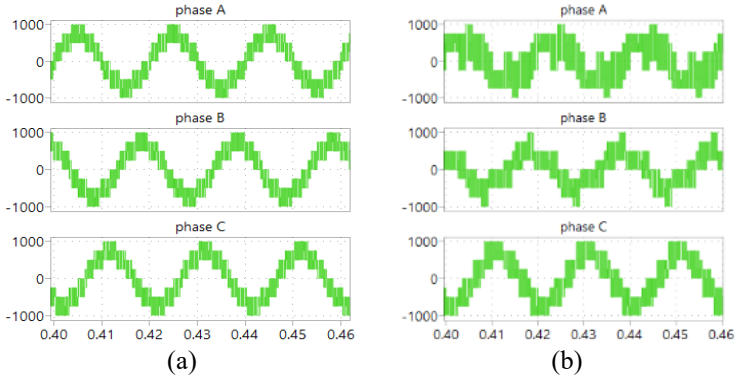
Surveying with the same CPWM control technique, with a modulation index m = 0.8, the difference in output voltage is clearly shown in Figures 7 and 8. NPC inverter Figure 6 illustrates the voltage waveform of a 3-phase NPC inverter during an open circuit fault.



Figures 7. Open circuit fault in 3-phase NPC inverter

Figures 7(a) The phase voltage waveforms A, B, C still have 5 voltage levels (-1000V, -500V, 0V, 500V, 1000V). This shows that the multi-level structure of the NPC is still in normal (no fault) state.

Figure 7(b) Open circuit fault in a traditional NPC inverter causes voltage imbalance, specifically phase A loss, exacerbating output voltage distortion. T-NPC inverter Figure 7 illustrates the voltage waveform of a 3-phase T-NPC inverter when an open circuit fault occurs on the T branch.



Figures 8. Open circuit fault in branch T on 3-phase T-NPC inverter

Figures 8(a) shows a waveform similar to NPC. This technique generates 9 application voltage levels at adjustment number m=0.5.

Figures 8(b) failure of the T-branch valve in the open circuit has little effect on the peak amplitude of the output waveform.

The most distinct difference between the NPC and T-NPC inverters under the same control conditions m=0.8 during an open-circuit fault is the degree of waveform distortion. Both exhibit output voltage distortion, but an open-circuit fault in the conventional NPC inverter typically results in a greater overall distortion, notably causing severe degradation of voltage quality due to phase. The T-NPC inverter, specifically when the open-circuit fault occurs in the T-branch, demonstrates a better ability to maintain the peak output voltage magnitude compared to the NPC, although the fault still leads to increased harmonics and imbalance. An open-circuit fault in the NPC impacts the ability to generate all voltage levels comprehensively. In contrast, an open-circuit fault in the T-branch of the T-NPC primarily affects the ability of that phase to generate the zero-voltage level, while maintaining good overall voltage magnitude

4.3. Proposes the FPWM based FTC method

The proposed FPWM technique for the T-NPC inverter is shown in Figure 9, This is an advanced solution, particularly suitable for medium and high-power applications.

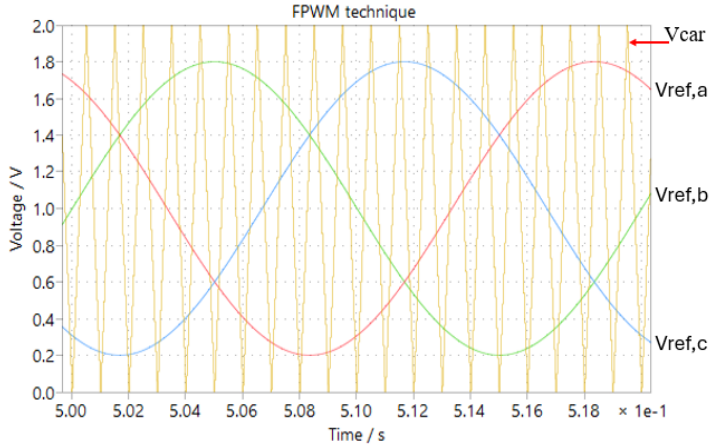
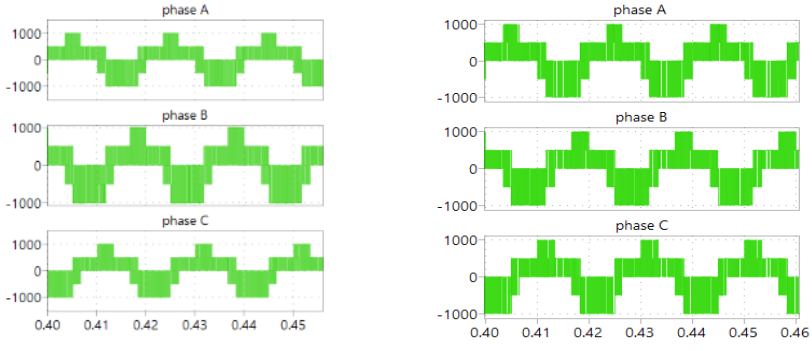


Figure 9. FPWM technique for T-NPC inverters

The FPWM technique in Figure 9 uses a Vcar wave compared with a Vref,x wave to produce a control signal for the corresponding IGBT switches on the T-NPC inverter.



(a) (b)

Figures 10. Output voltage waveform of the FPWM technique on the T-NPC inverter.

The re-analysis confirms that the waveforms in both Figures 10(a) and 10(b) exhibit five distinct voltage levels with a maintained peak magnitude of approximately $\pm$ 1000V

Figures 10(b) is important because it demonstrates the effectiveness of the proposed FPWM-based Fault Tolerant Control method. This technique is designed so that the inverter remains operational when an open circuit fault is detected in the T-branch of the T-NPC inverter with permissible amplitude and total THD distortion.

5. CONCLUSION

This research conducted an in-depth analysis of the thermal performance and open-circuit fault tolerance of the three-level T-Type Neutral Point Clamped inverter, as applied in the power conversion system of a wind energy conversion system. The power loss analysis, encompassing both conduction and switching losses under the Carrier-Based PWM strategy, demonstrates the T-NPC superior efficiency. Specifically, the T-NPC topology exhibits lower total power losses compared to the conventional Neutral Point Clamped (NPC) inverter across the linear modulation range. This advantage mainly stems from the reduction in overall switching losses, as the inner T-branch switches commute only across $V_{DC}/2$. However, the study also confirmed the T-NPC challenge of uneven thermal distribution across its components. The analysis of the open-circuit fault impact at the T-branch was conducted to assess reliability. Results indicated that the T-NPC has a better capability to maintain the output voltage peak magnitude compared to the traditional NPC when subjected to a fault. To enhance system reliability, the research proposed a Fault-Tolerant Control method based on PWM. This proposed strategy enables the T-NPC system to sustain continuous operation with maintained amplitude and acceptable output harmonic quality upon the detection of an OCF in the T-branch.

In summary, these findings not only validate the efficiency benefits of the T-NPC but also provide a robust FTC strategy, thereby contributing crucial data for the selection and design of highly efficient and reliable three-level inverters for renewable energy applications.

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