DOI: https://doi.org/10.62985/j.huit_ojs.vol26.no2E.378

A NON-ISOLATED ZETA-BOOST INTEGRATED DC-DC CONVERTER WITH REDUCED SWITCH STRESSES

Khai-Dat Nguyen, Hao-Dinh Vinh-Le, Van-Ban Nguyen,
Thanh-Hai Quach, Nghi-Vo Hong-Pham, Viet-Anh Truong*
Ho Chi Minh City University of Technology and Engineering, Ho Chi Minh City, Vietnam
*Email: *anhtv@hcmute.edu.vn*

Received: 16 January 2026; Revised: 16 March 2026; Accepted: 25 March 2026

ABSTRACT

This paper presents a novel non-isolated buck-boost DC power converter topology derived from the integration of the Zeta and Boost converter topologies, which is capable of smooth transition between step-down and step-up operating modes while providing an extended voltage conversion range. By analyzing the converter operation in CCM, closed-form expressions for the voltage conversion ratio, current sharing, and semiconductor stresses are obtained using volt–second and charge balance conditions. To improve input-side performance, an LC input filter is systematically designed according to the Middlebrook impedance criterion, effectively reducing switch current ripple and electromagnetic interference (EMI) without degrading the converter's dynamic characteristics. In addition, a small-signal model is developed for transfer function analysis and proportional–integral (PI) controller design, ensuring robust closed-loop stability with adequate gain and phase margins. Comparative evaluations and comprehensive simulations carried out in MATLAB/Simulink and PSIM confirm the analytical framework and the performance merits of the presented system.

Keywords: Step-up/step-down dc-dc converter, reduced voltage stress, non-isolated, large voltage conversion ratio.

1. INTRODUCTION

Electric energy is essential to modern industrial and socio-economic development, and environmental concerns have accelerated the integration of renewable-based power systems. Technologies such as PEMFC, EV, charging infrastructure and photovoltaic (PV) generators have attracted considerable attention due to their sustainability, low environmental impact, and suitability for decentralized power generation. However, the output voltage of most RES is low and highly variable (12 – 70 VDC) [1], requiring an efficient DC–DC conversion stage to regulate and boost the voltage for high-voltage loads or inverters [2], [3]. From a structural perspective, DC–DC converter architectures are generally divided into two primary categories: those with and without galvanic isolation. Despite the inherent advantage of galvanic isolation, isolated converters typically involve additional magnetic elements, which increase system complexity, power losses, and overall cost [4], [5]. When isolation is not required, non-isolated converters are preferred due to their compact structure, high power density, and high efficiency [6].

In RES-based systems, wide input-voltage variation limits the applicability of standard converters owing to their limited voltage conversion ratio, narrow duty-cycle range, and reduced efficiency under extreme operating conditions [7]. Consequently, high-gain and second-order converters based on switched-inductor/capacitor networks and hybrid boosting

techniques have been proposed [8]-[10]. Although Cúk, SEPIC, and Zeta converters offer continuous currents, their voltage gain remains insufficient for high step-up applications, while the topology in [11] improves voltage gain at the expense of increased component count and cost. The topology in [12] delivers a large voltage gain but suffers from output-voltage polarity reversal, higher device stress, and large current ripple, whereas other improved structures reduce device stress [13], [14] at the cost of reduced voltage gain or increased circuit complexity. To overcome limitations of existing designs, this work presents a new topology with enhanced voltage conversion ratio over [13], [14] and non-inverting output polarity compared to [12]. The key advantages are listed below:

- Wide operating range
- Reduced voltage and current stress on the switches
- Enhanced operating stability
- An LC input filter is designed to suppress source-side current fluctuations.

2. PROPOSED TOPOLOGY

As illustrated in Fig. 1, the proposed converter is derived from the integration of the Zeta and Boost converter topologies in order to achieve high voltage gain while reducing current and voltage stress on the components, which comprises a pair of inductors and capacitors, along with a pair of power switches and diodes. The power switches are operated in a synchronous manner, whereas the diodes remain reverse-biased during the on-state of the switches. Appropriate selection of inductance and capacitance ensures CCM operation, under which the capacitor voltages are assumed constant. The detailed operating principles and corresponding modes are presented in the following subsections.

2.1. Operating modes

Mode 1 $\left(0 \le t \le \mathrm{DT_s}\right)$: $\mathrm{S_1}$, $\mathrm{S_2}$ are gated on simultaneously, energy is initially supplied by the input source to the inductors $\mathrm{L_1}$ and $\mathrm{L_2}$, resulting in linearly increasing inductor currents due to the applied positive voltages. During this interval, diodes $\mathrm{D_1}$ and $\mathrm{D_2}$ are reverse-biased. Meanwhile, the capacitor $\mathrm{C_1}$ is charged, whereas the capacitor $\mathrm{C_2}$ supplies its stored energy to the load.

Mode 2 $\left(\mathrm{DT_s} \le t \le \mathrm{T_s}\right)$: Both switches are gated off, and the stored energy in $\mathrm{L_1}$ is transferred to $\mathrm{C_1}$, causing its current to decrease linearly, while $\mathrm{C_2}$ is charged. Under this condition, $\mathrm{D_1}$ and $\mathrm{D_2}$ are forward-biased. Meanwhile, the current in the inductor $\mathrm{L_2}$ remains continuous and supplies the load. In this operating mode, both inductors experience negative voltages, resulting in negative current slopes.

These relationships are obtained from the above analysis and expressed in (1).

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = D(V_{in}) + (1-D)(v_{C_1});\ L_2 \dfrac{di_{L_2}}{dt} = D(V_{in} - v_{C_1}) - (1-D)(v_o) \\ C_1 \dfrac{dv_{C_1}}{dt} = D(i_{L_2}) - (1-D)(i_{L_1});\ C_2 \dfrac{dv_{C_2}}{dt} = -D(I_o) + (1-D)(i_{L_2} - I_o) \end{cases} \quad (1)$$

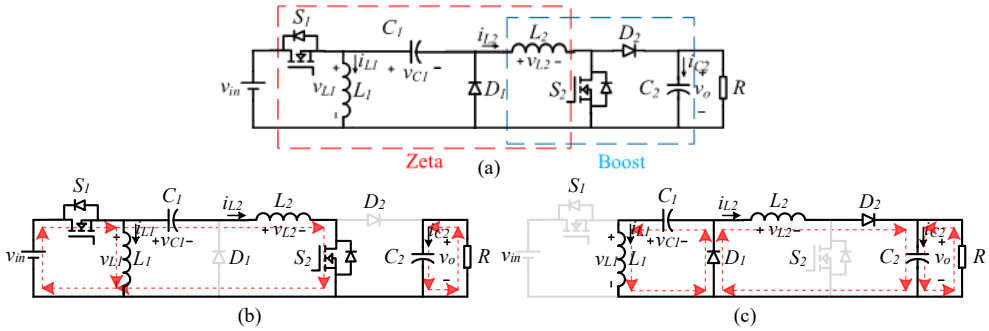

Fig.1. (a) Proposed topology, (b) Mode 1, (c) Mode 2.

2.2. Volt-Second Balance

The inductors must satisfy the volt-second balance condition in order to achieve steady-state operation. If this condition is not met, the inductor's current will continuously increase in an unbalanced manner, which may lead to inductor saturation and eventual damage. Under steady-state operation, each inductor satisfies the zero average voltage condition over one switching cycle. Accordingly, the inductor voltage expressions in (1) are equated to zero, from which the average capacitor voltages are derived as given in (2).

$$V_{C_1} = \frac{-DV_{in}}{1-D},\ V_{C_2} = V_o,\ V_o = \frac{D}{(1-D)^2}V_{in} \tag{2}$$

From (2), the voltage conversion ratio of the converter can be determined as

$$M_{CCM} = \frac{V_{out}}{V_{in}} = \frac{D}{(1-D)^2} \tag{3}$$

Based on (3), the step-up mode and step-down mode operations occur when D > 0.38 and D < 0.38, respectively.

2.3. Charge-Second Balance

At steady state, charge balance ensures that the capacitors have zero average current over a switching cycle. As a result, the average inductor currents are derived as given in (4).

$$I_{L_1} = \frac{DI_o}{(1-D)^2};\ I_{L_2} = \frac{I_o}{1-D} \tag{4}$$

2.4. Voltage/Current Stresses

The voltage stresses on S_1, S_2, D_1 and D_2 are expressed as (5).

$$V_{S_1} = \frac{V_{in}}{1-D};\ V_{S_2} = V_{out};\ V_{D_1} = -V_{in} + V_{C_1} = \frac{-DV_{in}}{1-D};\ V_{D_2} = -V_{out} = -\frac{D}{(1-D)^2}V_{in} \tag{5}$$

Using (4), the average currents across S_1, S_2, D_1 and D_2 are following as

$$\begin{cases} I_{S_1} = D(I_{L_1} + I_{L_2}) = \dfrac{DI_0}{(1-D)^2};\ I_{S_2} = DI_{L_2} = \dfrac{DI_o}{1-D} \\ I_{D_1} = (1-D)(I_{L_1} + I_{L_2}) = \dfrac{I_o}{1-D};\ I_{D_2} = (1-D)I_{L_2} = I_o \end{cases} \tag{6}$$

2.5. Inductor and Capacitor Ripple Analysis

The inductor current ripples are calculated using (1) and expressed in (7).

$$\Delta i_{L_1} = \frac{V_o(1-D)^2}{L_1 f_s};\ \Delta i_{L_2} = \frac{V_o(1-D)}{L_2 f_s};\ \Delta v_{C_1} = \frac{I_o D}{C_1(1-D) f_s};\ \Delta v_{C_2} = \frac{I_o D}{C_2 f_s} \tag{7}$$

To guarantee continuous conduction mode (CCM) operation, each inductor and capacitor must meet a minimum value determined by (7). Under the assumptions of $\Delta i_{L_1} \le x\% I_{L_1}$, $\Delta i_{L_2} \le x\% I_{L_2}$, $\Delta v_{C_1} \le y\% V_{C_1}$ and $\Delta v_{C_2} \le y\% V_{C_2}$, the corresponding inductance and capacitance requirements are given in (8).

$$L_1 > \frac{R(1-D)^4}{x\%2Df_s};\ L_2 > \frac{R(1-D)^2}{x\%2f_s};\ C_1 > \frac{D}{y\%2R(1-D)^2 f_s};\ C_2 > \frac{D}{y\%2Rf_s} \tag{8}$$

2.6. Efficiency Analysis

The efficiency can be expressed as follows:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_L + P_C + P_S + P_D} \tag{9}$$

with

$$P_S = \left(\frac{Dr_{S_1}}{(1-D)^4 R} + \frac{Dr_{S_2}}{(1-D)^2 R} \right) P_o + \left(f_S \frac{(t_{r_1} + t_{f_1}) + D(t_{r_2} + t_{f_2})}{2D(1-D)} \right) P_o \tag{10}$$

$$P_L = a_1 B_1^b f_1^c l_{m_1} A_{c_1} + a_2 B_2^b f_2^c l_{m_2} A_{c_2} + \left(\frac{r_{L_1} D^2}{(1-D)^4 R} + \frac{r_{L_2}}{(1-D)^2 R} \right) P_o \tag{11}$$

$$P_C = \left(\frac{Dr_{C_1}}{(1-D)^3 R} + \frac{Dr_{C_2}}{(1-D)R} \right) P_o;\ P_D = \left[\frac{V_{F_1}}{(1-D)V_{out}} + \frac{V_{F_2}}{V_{out}} + \frac{r_{D_1}}{(1-D)^3 R} + \frac{r_{D_2}}{(1-D)R} \right] P_o \tag{12}$$

3. SMALL SIGNAL ANALYSIS

To examine the topology dynamics, a linearized representation is formulated in this part, from which the duty–to–output dynamics is obtained for subsequent controller design. The corresponding Bode diagrams are subsequently obtained through MATLAB simulations. To facilitate linearization of the system equations, small perturbations are introduced to the state variables as follows:

$$\begin{cases} d = D + \hat{d} \\ v_{in} = V_{in} + \hat{v}_{in};\ v_{out} = V_{out} + \hat{v}_{out} \\ v_{C_1} = V_{C_1} + \hat{v}_{C_1};\ v_{C_2} = V_{C_2} + \hat{v}_{C_2} \\ i_{L_1} = I_{L_1} + \hat{i}_{L_1};\ i_{L_2} = I_{L_2} + \hat{i}_{L_2} \end{cases} \tag{13}$$

Where the $\hat{x}$ denote small-signal perturbations of the variables, and the corresponding uppercase symbols represent their steady-state (DC) values, which are significantly larger than the perturbations. From (1) and (13), the resulting small-signal model can be expressed as follows:

$$\begin{cases} L_1\langle\dfrac{d\hat{i}_{L_1}}{dt}\rangle = \hat{d}V_{in} + \hat{D}v_{in} + (1-D)\hat{v}_{C_1} - \hat{d}V_{C_1} \\ L_2\langle\dfrac{d\hat{i}_{L_2}}{dt}\rangle = D\hat{v}_{in} + \hat{d}V_{in} - D\hat{v}_{C_1} - \hat{d}V_{C_1} - (1-D)\hat{v}_{out} + \hat{d}V_{out} \\ C_1\langle\dfrac{d\hat{v}_{C_1}}{dt}\rangle = D\hat{i}_{L_2} + \hat{d}I_{L_2} - (1-D)\hat{i}_{L_1} + \hat{d}I_{L_1} \\ C_2\langle\dfrac{d\hat{v}_{C_2}}{dt}\rangle = (1-D)\hat{i}_{L_2} - \hat{d}I_{L_2} - \dfrac{\hat{v}_{out}}{R} \end{cases} \tag{14}$$

A state-space description corresponding to (14) is given by:

$$\frac{dx(t)}{dt} = x'(t) = Ax(t) + Bu(t),\ y(t) = Cx(t) + Du(t) \tag{15}$$

With

$$x(t) = \begin{bmatrix} \hat{i}_{L_1} & \hat{i}_{L_2} & \hat{v}_{C_1} & \hat{v}_{C_2} \end{bmatrix}^T;\ u(t) = \begin{bmatrix} \hat{v}_{in} & \hat{d} \end{bmatrix}^T;\ y(t) = \begin{bmatrix} v_{out} \end{bmatrix} = \begin{bmatrix} v_{C_2} \end{bmatrix} \tag{16}$$

Such that

$$\frac{dx(t)}{dt} = \begin{bmatrix} \dfrac{d\hat{i}_{L_1}}{dt} & \dfrac{d\hat{i}_{L_2}}{dt} & \dfrac{d\hat{v}_{C_1}}{dt} & \dfrac{d\hat{v}_{C_2}}{dt} \end{bmatrix}^T \tag{17}$$

The matrices A and B represent the state-space formulation containing the complete set of differential equations and are expressed as

$$A = \begin{bmatrix} 0 & 0 & \dfrac{1-D}{L_1} & 0 \\ 0 & 0 & \dfrac{-D}{L_2} & \dfrac{D-1}{L_2} \\ \dfrac{D-1}{C_1} & \dfrac{D}{C_1} & 0 & 0 \\ 0 & \dfrac{1-D}{C_2} & 0 & \dfrac{-1}{RC_2} \end{bmatrix};\ B = \begin{bmatrix} \dfrac{D}{L_1} & \dfrac{V_{in} - V_{C_1}}{L_1} \\ \dfrac{D}{L_2} & \dfrac{V_{in} - V_{C_1} + V_{C_2}}{L_2} \\ 0 & \dfrac{I_{L_1} + I_{L_2}}{C_1} \\ 0 & \dfrac{-I_{L_2}}{C_2} \end{bmatrix} \tag{18}$$

The matrices C and D are constructed to relate the output y(t) to the state vector x(t) and the input u(t), given as

$$C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix};\ D = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{19}$$

By transforming (14) into the Laplace domain, the duty–to–output dynamics is expressed as (20):

$$G(s) = C(sI - A)^{-1}B + D = \begin{bmatrix} \dfrac{\hat{v}_{out}}{\hat{v}_{in}} & \dfrac{\hat{v}_{out}}{\hat{d}} \end{bmatrix} \tag{20}$$

From (20), the control-to-output transfer function is expressed in (21).

$$G_{vd}(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{21}$$

Where

$$\begin{cases} a_0 = R(1-4D+6D^2-4D^3+D^4) \\ a_1 = D^2L_1 + L_2(1-2D+D^2) \\ a_2 = R(C_1L_1 - 2C_1DL_1 + C_1D^2L_1 + C_2D^2L_1 + C_2L_2 - 2C_2DL_2 + C_2D^2L_2) \\ a_3 = C_1L_1L_2 \\ a_4 = C_1\ C_2\ L_1\ L_2\ R \end{cases} \tag{22}$$

$$\begin{cases} b_0 = R(-V_{C_1} + 2DV_{C_1} - D^2V_{C_1} + V_{C_2} - 3DV_{C_2} + 3D^2V_{C_2} - D^3V_{C_2} + V_{in} - 2DV_{in} + D^2V_{in}) \\ b_1 = R(-DI_{L_1}L_1 + D^2I_{L_1}L_1 - DI_{L_2}L_1 - I_{L_2}L_2 + 2DI_{L_2}L_2 - D^2I_{L_2}L_2) \\ b_2 = R(-C_1L_1V_{C_1} + C_1D\ L_1V_{C_1} + C_1\ L_1V_{C_2} - C_1DL_1V_{C_2} + C_1L_1V_{in} - C_1DL_1V_{in}) \\ b_3 = -C_1I_{L_2}L_1L_2R \end{cases} \tag{23}$$

In this study, a PI controller is employed due to its ability to eliminate steady-state error through integral action and enhance dynamic response via the proportional term, while retaining a simple and practical structure. Although the cutoff frequency is generally selected to be at least one order of magnitude lower than the switching frequency, the transfer function in (20) exhibits resonant frequencies at 631 rad/s and 3245 rad/s. Therefore, a cutoff frequency of $\omega_c = 150$ rad/s, approximately 24% of the lowest resonant frequency, is chosen to ensure sufficient gain attenuation before the resonant region while maintaining acceptable transient performance.

The PI transfer function is expressed as

$$H(s) = K_p + \frac{K_I}{s} \tag{24}$$

The controller gains K_p and K_I are calculated using the following equations

$$\begin{cases} \left|H(j\omega)G(j\omega)\right| = 1 \\ 180° + \angle H(j\omega)G(j\omega) = PM \end{cases} \tag{25}$$

From (24), (25), and $\omega_c = 150$ rad/s, $PM = 70°$, K_p and K_I are calculated as

$$\begin{cases} K_P = 3.4\times10^{-5} \\ K_I = 0.49 \end{cases} \tag{26}$$

As shown in Fig. 2(a), the introduction of the PI controller significantly reduces the open-loop gain magnitude across the frequency range, achieving a gain margin of approximately 8.36 dB and a phase margin of about 70°, which satisfy the Bode stability criteria and indicate strong robustness against oscillations and parameter variations. Fig. 2(b) shows a transient response time of approximately 0.035s, representing a reasonable trade-off between stability and dynamic performance. Furthermore, the steep high-frequency magnitude roll-off effectively attenuates switching ripple and noise. These results confirm that the proposed PI controller ensures closed-loop stability and significantly enhances the robustness and control performance of the DC–DC converter.

4. SOLUTION FOR REDUCING THE INPUT CURRENT

In the proposed structure, the presence of a series-connected switching device leads to a pulsating input current at high switching frequencies, giving rise to considerable input current ripple and source-side conducted EMI. Although the inherent impedance of practical power sources can partially attenuate these disturbances, such attenuation is neither frequency-selective nor efficient and is often accompanied by additional power losses. To suppress high-frequency input current components without affecting the steady-state behavior of the DC source, an LC filter is introduced at the converter input, as shown in Fig. 3(a), whose cutoff frequency is set far below the switching frequency f_s in accordance with the design constraint given in (27).

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \le (0.05 \sim 0.1) f_s \tag{27}$$

Based on Middlebrook's impedance criterion, the effect of the input LC filter on the duty-to-output transfer function is expressed as

$$G_{vd}(s) = (G_{vd}(s)|_{Z_o(s)=0}) \frac{1 + \dfrac{Z_o(s)}{Z_N(s)}}{1 + \dfrac{Z_o(s)}{Z_D(s)}} \tag{28}$$

Here, $Z_o(s)$ refers to the output impedance of the input filter, $Z_N(s)$ denotes the incremental input driving-point impedance of the converter and $Z_D(s)$ corresponds to the null driving-point impedance. Based on Middlebrook's impedance criterion, the input filter is designed such that its output impedance satisfies the required stability condition.

$$|Z_o| \ll |Z_N|; \ |Z_o| \ll |Z_D| \tag{29}$$

Under closed-loop conditions, the input impedance of the converter is described by the following expression:

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1+T(s)} + \frac{1}{Z_D(s)} \frac{1}{1+T(s)} \tag{30}$$

Where $T(s)$ denotes the controller loop gain. At low frequencies, where the loop gain magnitude is large (hence $T \gg 1$), the regulator input impedance exhibits a negative-resistance characteristic and follows $Z_N(s)$ so that $|Z_o| \ll |Z_i|$. In this operating region, the converter behaves as a constant power source, so Z_i can be calculated as:

$$|Z_{in}| = \frac{V_{in}^2}{P_o} \tag{31}$$

In this study, $Z_o(s)$ is set to be more than twenty times smaller than $Z_i(s)$ in order to mitigate the influence of model uncertainties, at $f_{LC} = 5kHz$, $|Z_o(s)| \approx \omega L_f$, the component parameters are $L_f = 1\mu H$, $C_f = 1000\mu F$.

As illustrated in Fig. 3(b), the insertion of the LC filter significantly reduces the input current ripple compared with the unfiltered case, demonstrating its effectiveness in suppressing high-frequency switching components and conducted EMI. Consequently, the

input current becomes smoother, improving source quality and system stability. In addition, Fig. 2(a) shows that the system transfer function remains nearly unchanged after filter insertion, indicating a negligible impact on system dynamics. Therefore, the designed LC filter meets the required performance criteria.

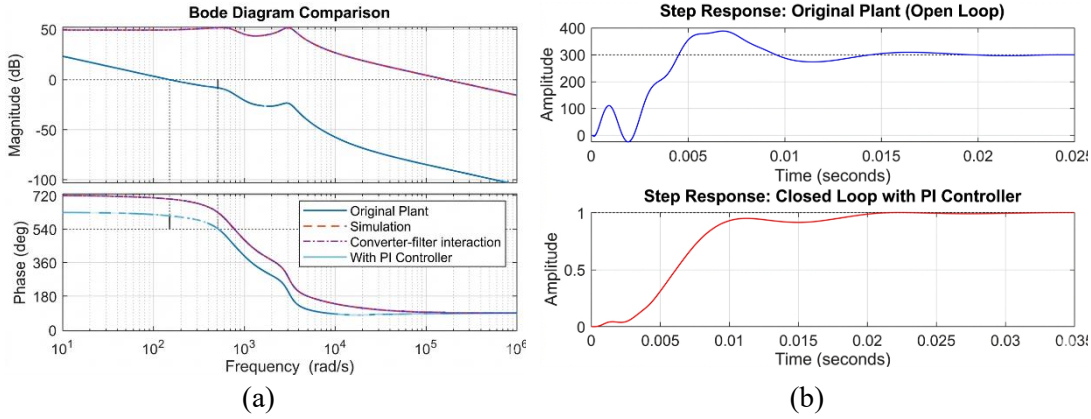

Fig.2. (a) Bode diagram with and without PI controller, (b) Step responses of the system before and after PI control.

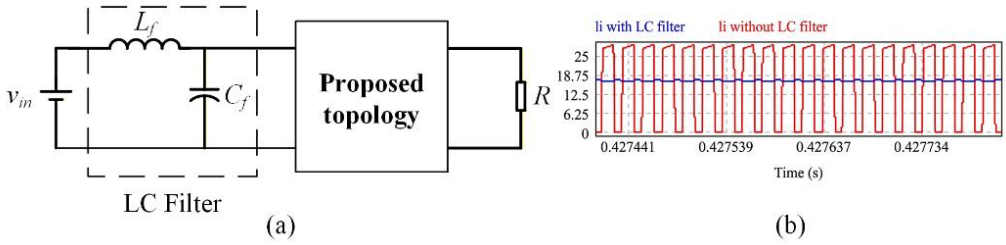

Fig.3. (a) The topology with LC filter, (b) Input current waveforms pre- and post-LC filter.

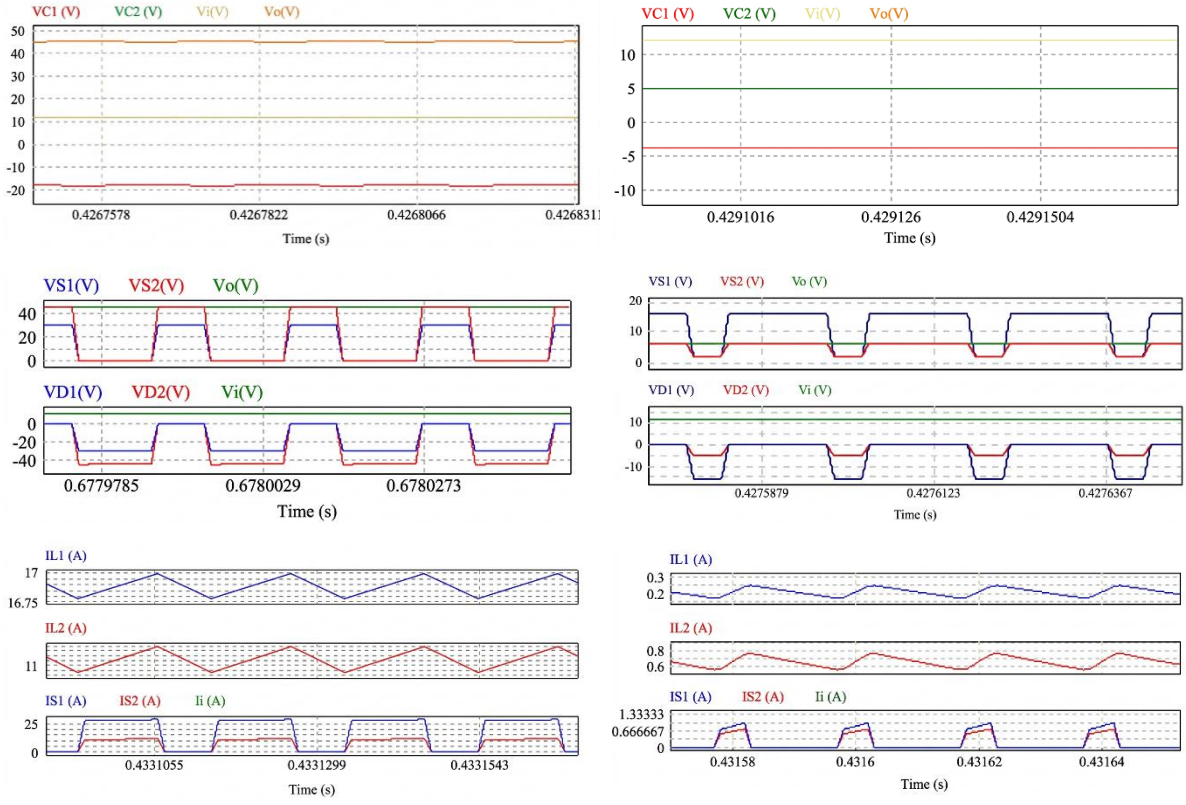

Fig.4. Simulation results: (a) Step-up mode, (b) Step-down mode.

5. SIMULATION RESULTS

Under a fixed 12 V supply, the proposed topology achieves regulated output voltages of 45 V in step-up condition and 5 V in step-down condition. The switching frequency is set to 50 kHz. Inductor values of 680 µH (L_1) and 330 µH (L_2) are selected using (4) and (8), while capacitor values of 390 µF (C_1) and 68 µF (C_2) are obtained from (2) and (8). Under step-up operation with a duty cycle of 60%, Fig. 4(a) presents the simulated waveforms, showing that the output voltage is regulated at 45 V from a 12 V input and the converter operates in CCM. The capacitor voltages of −18 V (C_1) and 44.9 V (C_2) closely match the theoretical predictions of (2). The average inductor currents are measured as 16.9 A for i_{L1} and 11.3 A for i_{L2}, in good agreement with (4). Moreover, the voltage stresses across S_1, S_2, D_1, and D_2 are 29.2 V, 44.9 V, −17.6 V, and −44.9 V, respectively, consistent with (5), and the switch currents of 17 A and 6.8 A follow the analytical results in (6). Fig. 4(b) presents the simulated step-down operation at a duty cycle of 24.04%, demonstrating voltage regulation from 12 V to 5 V under CCM. The capacitor voltages of −3.8 V (C_1) and 4.99 V (C_2) closely match the analytical predictions. The average inductor currents are 0.207 A (L_1) and 0.614 A (L_2), while the voltage stresses across S_1, S_2, D_1, and D_2 are 15.3 V, 4.99 V, −3.7 V, and −4.99 V, respectively. The corresponding switch currents of 0.75 A and 0.56 A further confirm the validity of the theoretical analysis.

6. COMPARISON WITH EXISTING TOPOLOGIES

Table I and Fig. 5 show a comparison between the structure proposed in this paper with other two-switch topologies under a 45 V output voltage, 50 kHz switching frequency, 10 Ω

load. The proposed structure uses fewer components than [13] and achieves a higher voltage gain than [13], [14], which is illustrated in Fig. 5(a). Although the voltage gain is lower than that of [12], it provides a non-inverting output. Furthermore, the voltage stresses on S_1, S_2 are reduced compared with [12]-[14]. The current stress on S1 is comparable to [13], [14] and lower than [12], S2 exhibits the lowest current stress among all converters in Table I.

Table 1. Comparison with other topologies

		Proposed	[12]	[13]	[14]
Elements	C	2	2	3	3
	D	2	2	2	2
	L	2	2	3	3
	S	2	2	2	2
M_{CCM}		$\frac{D}{(1-D)^2}$	$\frac{-D(2-D)}{(1-D)^2}$	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$
$\lvert V_{S_1} / V_{out}\rvert$		$\frac{1-D}{D}$	$\frac{-1}{D(2-D)^2}$	$\frac{1}{1-D}$	$\frac{1-D}{D^2}$
$\lvert V_{S_2} / V_{out}\rvert$		1	$\frac{-1}{D(2-D)}$	$\frac{D}{(1-D)^2}$	$\frac{1}{D}$
$\lvert I_{S_1} / I_{in}\rvert$		1	$\frac{-D^2(2-D)}{(1-D)^4}$	1	1
$\lvert I_{S_2} / I_{in}\rvert$		$D(1-D)$	$\frac{-D^2(2-D)}{(1-D)^3}$	$\frac{1-2D}{D}$	$\frac{1-D}{D}$

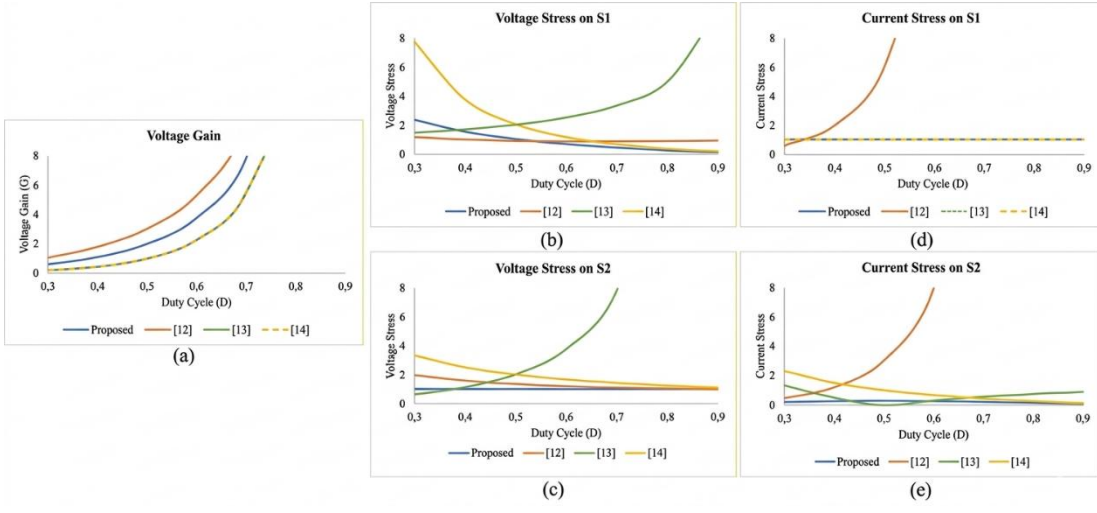

Fig.5. Comparison of: (a) Voltage gain, (b) Voltage stress on S_1, (c) Voltage stress on S_2, (d) Current stress on S_1, (e) Current stress on S_2.

7. CONCLUSION

This study introduces a non-isolated buck–boost DC–DC converter with high-gain step-up and step-down capability, non-inverting output polarity, while significantly alleviating the voltage and current stresses on the switches. Steady-state CCM characteristics, including voltage gain, current distribution, and device stresses, are analytically derived. A small-signal model and an LC input filter, based on Middlebrook's criterion, are developed to improve dynamic performance and reduce input-current ripple. Simulation results in MATLAB/Simulink and PSIM validate the theoretical analysis. Future work will focus on implementing a hardware prototype for experimental verification, developing a non-ideal small-signal model considering parasitic elements, and conducting efficiency comparisons with existing topologies.

Acknowledgment: The authors would like to thank Ho Chi Minh City University of Technology and Engineering, notably the Renewable Energy and Power Systems Laboratory (C201) and the Industrial System Registration Laboratory (C402), for providing essential facilities and technical support throughout this research, under project code SV2026-259.

REFERENCES

[1] T. Tomaszuk and A. Krupa, "High efficiency high step-up DC/DC converters-A review," *Bulletin of The Polish Academy of Sciences Technical Sciences*, vol. 59, no. 4, 2011, doi: https://doi.org/10.2478/v10175-011-0059-1.

[2] Y. Koc, Y. Birbir, and H. Bodur, "Non-isolated high step-up DC/DC converters - An overview," *Alex. Eng. J*, vol. 61, no. 2, pp. 1091-1132, doi: https://doi.org/10.1016/j.aej.2021.06.071.

[3] J. Bürger, A. Kersten, M. Kuder, R. Eckerle, T. Wehn, and T. Trumpp, "Total CO_2 equivalent life-cycle emissions from commercially available passenger cars," *Renew. Sustain. Energy Rev.*, vol. 159, Art. no. 112158, May 2022, doi: https://doi.org/10.1016/j.rser.2022.112158.

[4] R. Swarnkar and R. HariKrishnan, "Comparative analysis of transformerless bi-directional DC–DC converter and conventional converter for battery charging–discharging applications," *Recent Advances in Manufacturing, Automation, Design and Energy Technologies*, pp. 935–944, 2022, doi: https://doi.org/10.1007/978-981-16-4222-7_102.

[5] F. Mumtaz, N. Z. Yahaya, S. T. Meraj, B. Singh, R. Kannan, and O. Ibrahim, "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications," *Ain Shams Eng. J.*, vol. 12, pp. 3747–3763, 2021, doi: https://doi.org/10.1016/j.asej.2021.03.022.

[6] F. A. Abbas, T. A. Abdul-Jabbar, A. A. Obed, A. Kersten, M. Kuder, and T. Weyh, "A Comprehensive Review and Analytical Comparison of Non-Isolated DC-DC Converters for Fuel Cell Applications," *Energies*, vol. 16, no.8, Apr. 2023, doi: https://doi.org/10.3390/en16083493.

[7] J. L. Seguel, S. I. Seleme, and L. M. F. Morais, "Comparative Study of Buck–Boost, SEPIC, Cuk, and Zeta DC–DC Converters Using Different MPPT Methods for Photovoltaic Applications," *Energies*, vol. 15, no. 21, Oct. 2022, doi: https://doi.org/10.3390/en15217936.

[8] M. Shaabani, A. Mirzaei, M. Rezvanyvardom, F. Khosravi, and S. A. Gorji, "A hybrid switched-inductor/switched-capacitor DC–DC converter with high voltage gain using a

single switch for photovoltaic application," *Energies*, vol. 16, no. 14, Jul. 2023, Art. no. 5424, doi: https://doi.org/10.3390/en16145524.

[9] A. Imanlou, E. S. Najmi, R. Behkam, M. Nazari-Heris, and G. B. Gharehpetian, "A New High Voltage Gain Active Switched-Inductor Based High Step-Up DC–DC Converter with Coupled-Inductor," *IEEE Access*, Jun. 2023, doi: https://doi.org/10.1109/ACCESS.2023.3283471.

[10] Behdad Faridpak, Mohammad Bayat, Mojtaba Nasiri, Rahim Samanbakhsh, Meisam Farrokhifar, "Improved hybrid switched inductor/switched capacitor DC-DC converters", *IEEE Trans. Power. Electron.*, vol: 36, no. 3, pp. 3053-3062, Mar. 2021, doi: https://doi.org/10.1109/TPEL.2020.3014278.

[11] M. R. Banaei and H. A. F. Bonab, "A novel structure for single-switch nonisolated transformerless buck–boost DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 198–205, Jan. 2017, doi: https://doi.org/10.1109/TIE.2016.2608321.

[12] S. Ding and F. Wang, "A new negative output buck–boost converter with wide conversion ratio," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9322–9333, Dec. 2017, doi: https://doi.org/10.1109/TIE.2017.2711541.

[13] A. Sarikhani, B. Allahverdijejad, M. Hamzeh, and E. Afjei, "A continuous input and output current buck–boost converter with positive output voltage for photovoltaic applications," *Solar Energy*, vol. 188, pp. 19–27, 2019, doi: https://doi.org/10.1016/j.solener.2019.05.025.

[14] H. Gholizadeh, S. A. Gorji, and D. Sera, "A quadratic buck–boost converter with continuous input and output currents," *IEEE Access*, vol. 11, pp. 22376–22393, 2023, doi: https://doi.org/10.1109/ACCESS.2023.3253102.