DOI: https://doi.org/10.62985/j.huit_ojs.vol26.no2E.379

ENHANCED CONTROL OF FOUR-LEVEL NNPC INVERTER FOR MEDIUM-VOLTAGE DRIVE APPLICATIONS

Le Nam Pham[1,2,3*], Quoc Dung Phan[2,3], Van Nho Nguyen[2,3]

[1]*Eastern International University*

[2]*Ho Chi Minh City University of Technology*

[3]*Vietnam National University Ho Chi Minh City*

*Email: *nam.pham@eiu.edu.vn*

Received: 16 December 2025; Revised: 7 March 2026; Accepted: 9 April 2026

ABSTRACT

Multilevel inverters have been extensively employed in motor drive systems owing to their capability to produce high-quality output voltage waveforms, reduce dv/dt stress, and improve overall system efficiency. Among these, four-level topologies are particularly attractive for medium-voltage applications because of their superior waveform quality, higher voltage rating, and better suitability for high-power drives. However, conventional four-level inverters often suffer from capacitor voltage imbalance, which can significantly degrade output quality, induce harmonic distortion, and compromise drive reliability. The Four-level Nested Neutral-Point-Clamped (4L-NNPC) inverter has emerged as a promising solution, offering improved flying-capacitor (FC) voltage balancing under rated conditions. Nevertheless, maintaining stable FC voltages remains challenging under dynamic operating conditions, where irregular capacitor charging can lead to voltage drift, increased ripple, and higher common-mode voltage, thereby reducing the overall performance of the drive. Therefore, this paper proposes a high-performance control strategy to improve total harmonic distortion (THD) and reduce common-mode voltage (CMV) in a field-oriented control (FOC) medium-voltage induction motor drive fed by a 4LNNPC inverter. A voltage-balancing control scheme is integrated to regulate FC voltages across a wide range of operating conditions, ensuring reliable and efficient motor operation. Simulation results demonstrate the effectiveness of the proposed strategies compared to conventional methods, confirming enhanced voltage stability, lower THD, and reduced CMV, which collectively contribute to superior drive performance and robustness.

Keywords: Common-mode voltage, Field-oriented control, four-level inverter, pulse width modulation, total harmonic distortion (THD).

1. INTRODUCTION

Medium-voltage induction motor (IM) drives are widely employed in industrial applications, including pumps, fans, compressors, conveyors, and traction systems, due to their robustness, reliability, and cost-effectiveness [1]. With increasing demand for energy-efficient and high-performance industrial systems, medium-voltage drives are expected to deliver precise torque and speed control while minimizing power losses and voltage stress on electrical components [2], [3]. In this context, multilevel inverters (MLIs) have emerged as a key enabling technology, capable of generating high-quality voltage waveforms, reducing dv/dt stress on motor windings, lowering total harmonic distortion (THD), and minimizing switching losses compared to conventional two-level inverters [4], [5].

Over the past decades, various multilevel inverter topologies, including Neutral-Point-Clamped (NPC), Flying-Capacitor (FC), and Cascaded H-Bridge (CHB) inverters, have been extensively studied [4], [5]. For medium-voltage drives, three-level NPC (3L-NPC) inverters are commonly employed, offering a good compromise between complexity and performance [2]. As voltage requirements increase, four-level (4L) inverter topologies have attracted attention due to their superior output voltage quality, extended voltage range, and reduced stress on switching devices. However, the conventional four-level NPC inverters often suffer from DC-link capacitor voltage imbalance, which can degrade stator current quality, increase harmonic content, and compromise drive reliability [6].

Recently, the four-level Nested Neutral-Point-Clamped (4L-NNPC) inverter combines the advantages of NPC and FC topologies, introducing redundant switching states that facilitate effective flying-capacitor (FC) voltage balancing and maintain high-quality voltage waveforms [7]. Despite the aforementioned merits, the industrial adoption of the 4L-NNPC remains challenged by technical issues. One of the technical issues lies in maintaining stable FC voltages across a low-speed operation, and the requirement of reducing common-mode voltage (CMV). The conventional space vector modulation (SVM) [8] the sinusoidal pulse width modulation (SPWM) [9], and the space virtual-vector modulation (SVVM) [10] have been introduced to control the FCs' voltages. These methods are effective at the fundamental frequency but suffer from serious voltage imbalance at low output frequencies. To get a complete control of FC's voltages, advanced VBC methods have been investigated [11]. However, the use of redundant states, multiple switching actions, as well as virtual or distant vectors significantly deteriorates the total harmonic distortion and increases switching losses. Moreover, they also result in a high CMV, which is undesirable in many industrial applications. The work in [12] proposed a method for the 4L-NNPC inverter that minimizes the peak CMV to $\pm V_d/18$, while [13] introduced an average zero-CMV (AZCMV) PWM technique based on virtual vectors to reduce low-frequency CMV in four-level NPC inverters. However, both methods rely heavily on distant space vectors, which inherently deteriorates the output harmonic quality and leads to relatively high THD. Moreover, neither approach incorporates a dedicated flying-capacitor or DC-link voltage-balancing strategy, making them unsuitable for applications where stable capacitor voltages and high-quality waveforms are required. Similarly, the works in [14], [15] present the carrier-based discontinuous PWM methods that restrict the CMV to $\pm V_d/6$; however, the issue of floating capacitor voltage balancing is also not addressed, which limits the applicability of these methods in medium-voltage drive systems.

To overcome these limitations, this paper proposes a high-performance control strategy for a medium-voltage IM drive fed by a 4L-NNPC inverter. A carrier-based PWM scheme is combined with FOC and a voltage-balancing control method to enhance voltage stability, reduce THD, suppress CMV, and improve overall drive efficiency. Unlike conventional PWM approaches that mainly focus on steady-state performance or treat FC voltage balancing and CMV reduction separately, the proposed method introduces an integrated control that simultaneously achieves dynamic FC voltage regulation and CMV suppression over a wide operating range. The proposed strategy offers a practical solution for industrial medium-voltage drives, ensuring reliable, efficient, and high-performance operation.

The main contributions of this work can be summarized as follows:

- Development of a high-performance control strategy for a medium-voltage induction motor (IM) drive fed by a four-level Nested Neutral-Point-Clamped (4L-NNPC) inverter, integrating field-oriented control (FOC) for precise torque regulation.

- Introduction of a carrier-based pulse-width modulation (PWM) scheme that effectively reduces total harmonic distortion (THD) and suppresses common-mode voltage (CMV), enhancing overall drive efficiency and reliability.
- Implementation of a voltage-balancing control method to maintain stable flying capacitor (FC) voltages across various operating conditions, preventing voltage drift and ensuring high-quality output waveforms.
- Comprehensive simulation-based validation comparing the proposed approach with conventional PWM and control techniques, demonstrating significant improvements in voltage stability, current quality, harmonic reduction, and overall drive performance.

The remainder of the paper is organized as follows. Section 2 presents the modeling of the four-level Nested Neutral-Point-Clamped (4L-NNPC) inverter and the medium-voltage induction motor (IM) drive system, including flying-capacitor voltage characteristics and the relevant mathematical formulations. Section 3 introduces the proposed high-performance control strategy, detailing the carrier-based pulse-width modulation (PWM) scheme, and the voltage-balancing method. Section 4 provides comprehensive simulation studies and performance analysis. Finally, Section 5 concludes the paper by summarizing the main findings and contributions and suggesting potential directions for future research.

2. FOUR-LEVEL NNPC INVERTER IN DRIVE SYSTEM

Fig. 1 shows the schematic diagram of the 4L-NNPC fed MV drive system. In which, the rectifier system of MV drive can be modeled as a DC voltage source with a constant value of V_d. Each phase of the inverter has six IGBT devices (S_{1x}-S_{6x}), two clamping diodes, and two flying capacitors ($x = a$, b, and c). The rated voltage of the flying capacitor is one-third of the DC-link voltage ($V_d/3$).

The switching state S_x of phase x is defined as:

$$S_x = S_{1x} + S_{2x} + S_{3x} \tag{1}$$

The output phase leg voltage is:

$$V_{x0} = \frac{V_d}{3} S_x \tag{2}$$

In 4L-NNPC inverter, four levels of phase leg voltage are generated: 0, $V_d/3$, $2V_d/3$, and V_d, where V_d represents the total DC-link voltage. The switching state function 2 includes two redundant states, 2a and 2b, while the switching state function 1 includes two redundant states, 1a and 1b [12]. Although these redundant switching states produce the same output voltage, they result in different device states, leading to varying impacts on the flying capacitor voltages, as demonstrated in Table 1.

Table 1. Switching states of 4L-NNPC inverter [12]

S_x	State	Device state						Flying capacitor voltage	
		S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}	V_{C1x}	V_{C2x}
3	3	1	1	1	0	0	0	No change	No change
2	2a	1	0	1	1	0	0	Charging (i>0) Discharging (i<0)	No change
	2b	0	1	1	0	0	1	Discharging (i>0) Charging (i<0)	Discharging (i>0) Charging (i<0)
1	1a	1	0	0	1	1	0	Charging (i>0) Discharging (i<0)	Charging (i>0) Discharging (i<0)

S_x	State	Device state						Flying capacitor voltage	
		S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}	V_{C1x}	V_{C2x}
	1b	0	0	1	1	0	1	No change	Discharging (i>0) Charging (i<0)
0	0	0	0	0	1	1	1	No change	No change

The inverter output currents, corresponding to the motor stator currents, are governed according to the motor flux and torque/speed through a field-oriented control (FOC) scheme. The overall control structure of the 4L-NNPC inverter-fed medium-voltage drive is illustrated in Fig. 2, where an indirect field-oriented control (IFOC) strategy is employed [16]. In this framework, the motor flux and speed are managed by the outer control loops, while the dq-axis components of the stator currents are regulated by the inner current controllers. The output of IFOC controller generate the stator reference voltages v_{as}, v_{bs}, v_{cs} for modulation scheme.

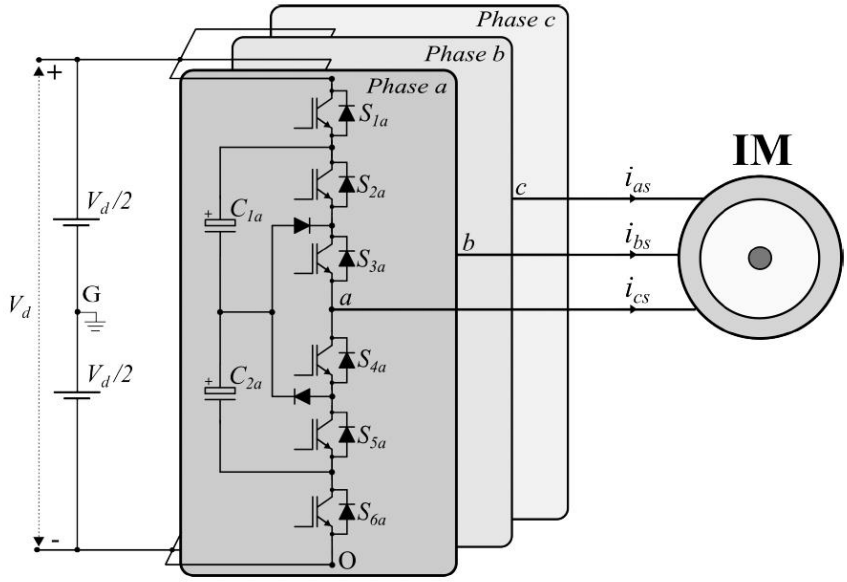

Fig. 1. The 4L-NNPC fed MV drive system

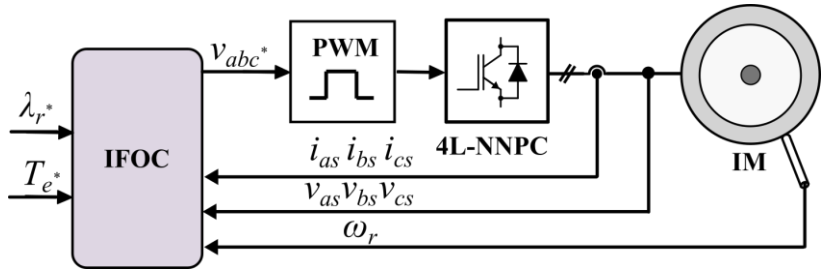

Fig. 2. Control system diagram of the 4L-NNPC inverter fed MV drive

The space vector diagram (SVD) of 4L-NNPC inverter can be deduced from:

$$\vec{S}(S_a, S_b, S_c) = \frac{2}{3}(S_a + \bar{a}S_b + \bar{a}^2 S_c) \qquad (3)$$

with $\bar{a} = e^{j2\pi/3}$. As illustrated in Fig. 3(a), there are 64 space vectors in the four-level SVD (4L-SVD) of 4L-NNPC inverter.

The common-mode voltage CMV (V_{cm}) is defined as the voltage between the neutral (N) and the middle point of the DC link source (G) [15]:

$$V_{cm} = \left[\frac{2}{9}(S_a + S_b + S_c) - 1\right]\frac{V_d}{2} = \left(\frac{2}{9}F - 1\right)\frac{V_d}{2} \quad (4)$$

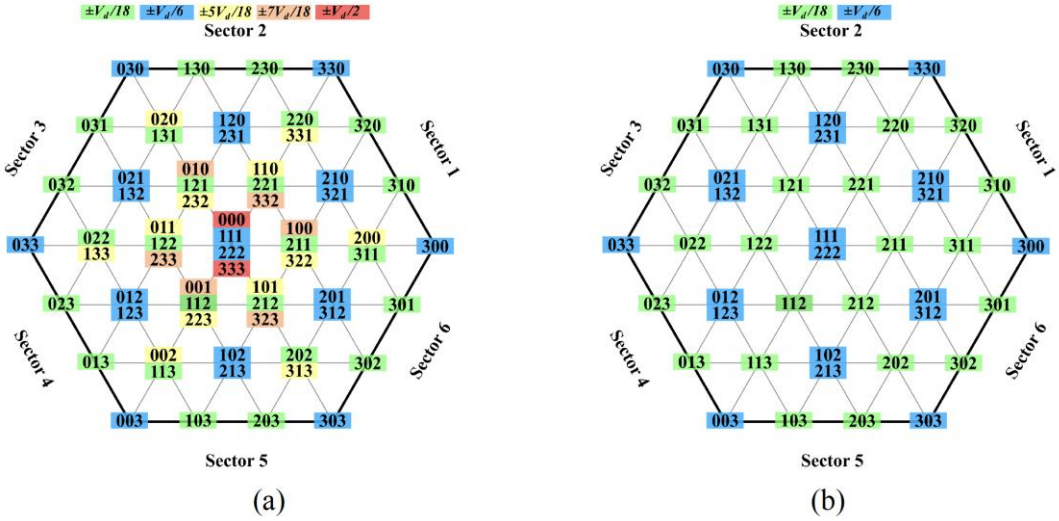

Fig. 3. (a) Full space vector diagram of 4L-NNPC inverter. (b) Reduced-CMV space vector diagram of 4L-NNPC inverter

where total switching function of a vector is defined as:

$$F = S_a + S_b + S_c \quad (5)$$

In (5), F is defined as the total switching function. All switching vectors, total switching functions and the corresponding CMV values can be listed in Table 2. In which, the reduced CMV (RCMV) vectors are defined as CMVs $-V_d/6$, $-V_d/18$, $+V_d/18$, and $+V_d/6$ [15], with the corresponding $F = \{3, 4, 5, 6\}$, as shown in the RCMV SVD in Fig. 3(b).

3. PROPOSED SCHEME

3.1. Carrier-based PWM Scheme for 4L-NNPC inverter

The average reference stator voltage vector $\overrightarrow{v_{ref}} = V_m e^{j\omega t}$ can be expressed in *abc* frame as follows:

$$V_x = \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos(\omega t - 2\pi/3) \\ V_m \cos(\omega t + 2\pi/3) \end{bmatrix} \quad (6)$$

Let N denote the motor neutral point, the average offset voltage V_{off} (V_{NO}) defined between points N and O, is added to the phase reference signals to obtain the average phase-leg voltages:

$$V_{xO} = \begin{bmatrix} V_{as} + V_{off} \\ V_{bs} + V_{off} \\ V_{cs} + V_{off} \end{bmatrix} \quad (7)$$

For carrier-based PWM in the 4L-NNPC inverter, these voltages are normalized by $V_d/3$, giving the reference control signals:

$$V_{xO} = \begin{bmatrix} V_{aref}.V_d/3 \\ V_{bref}.V_d/3 \\ V_{cref}.V_d/3 \end{bmatrix} \quad (8)$$

Thus, the normalized modulating signals become:

$$v_{xref} = \begin{bmatrix} v_{aref} \\ v_{bref} \\ v_{cref} \end{bmatrix} = \begin{bmatrix} v_{as} + v_{off} \\ v_{bs} + v_{off} \\ v_{cs} + v_{off} \end{bmatrix} = \begin{bmatrix} \sqrt{3}m\cos(\omega t) + v_{off} \\ \sqrt{3}m\cos(\omega t - 2\pi/3) + v_{off} \\ \sqrt{3}m\cos(\omega t + 2\pi/3) + v_{off} \end{bmatrix} \quad (9)$$

where $\{v_{as}, v_{bs}, v_{cs}\}$ are the normalized average reference stator voltages, and the modulation index *m* is:

$$m = \frac{V_m}{V_d/\sqrt{3}} \quad (10)$$

In a sampling period, v_{xref} is a constant and can be decomposed into two components: $\{L_a, L_b, L_c\}$ are the base voltages, and $\{e_a, e_b, e_c\}$ are the normalized average two-level switching voltages. The total base voltage (F_L) and total active voltage (F_E) in two-level space vector diagram (2L-SVD) are defined as:

$$F_L = L_a + L_b + L_c; F_E = e_a + e_b + e_c \quad (11)$$

For RCMV operation of the 4L-NNPC inverter, the total switching function must satisfy:

$$F = F_L + F_E = \{3,4,5,6\} \quad (12)$$

Accordingly, the four-level SVD is categorized into three RCMV-compatible 2L-SVD types:

• 2L-SVD Type 1 ($F_L = 4$): active vectors satisfied F_E = {0, 1, 2} ⇒ F = {4, 5, 6}.

• 2L-SVD Type 2 ($F_L = 2$): active vectors satisfied F_E = {1, 2, 3} ⇒ F = {3, 4, 5}.

• 2L-SVD Type 1 ($F_L = 3$): active vectors satisfied F_E = {0, 1, 2,3} ⇒ F = {3,4, 5, 6}.

As illustrated in Fig. 4, region identification is performed using (d_1): $mid - min = 2$, (d_2): $max - mid = 2$, and (d_3): $max - min = 1$, in which:

$$max = max(v_{as}, v_{bs}, v_{cs}); mid = mid(v_{as}, v_{bs}, v_{cs}); min = min(v_{as}, v_{bs}, v_{cs}) \quad (13)$$

These conditions divide the reference vector space into 13 regions, as illustrated in Fig. 4, with corresponding base vector assignments summarized in Table 2. Once the region and its associated SVD type are determined, the 2L switching components are computed as:

$$e_x = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \begin{bmatrix} v_{aref} - L_a \\ v_{bref} - L_b \\ v_{cref} - L_c \end{bmatrix} \quad (14)$$

The offset value is selected according to the SVD type:

• 2L-SVD Type 1 (F_L = 4): $e_o = -min(e_a, e_b, e_c)$.

• 2L-SVD Type 2 (F_L = 2): $e_o = 1 - max(e_a, e_b, e_c)$.

• 2L-SVD Type 1 (F_L = 3): $e_o = [min(e_a, e_b, e_c) + max(e_a, e_b, e_c)]/2$.

The modified 2L-modulating signals are then computed as:

$$e_{xref} = \begin{bmatrix} e_a + e_o \\ e_b + e_o \\ e_c + e_o \end{bmatrix} \quad (15)$$

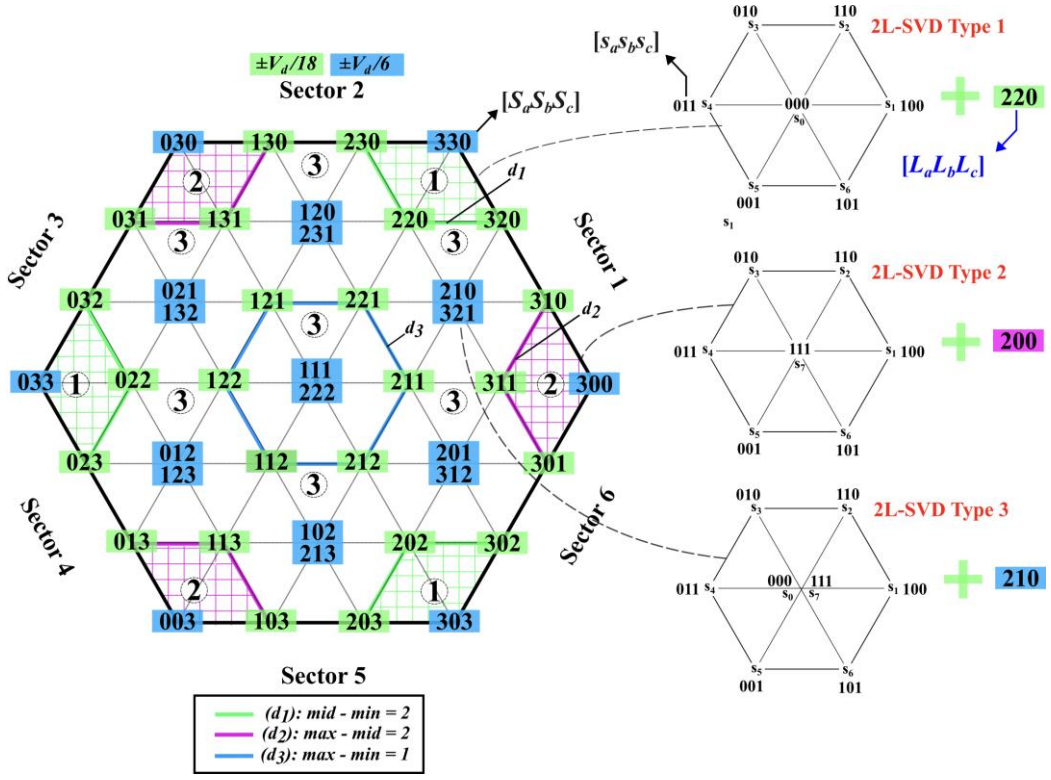

Fig. 4. Four-level to two-level transformation and region identification

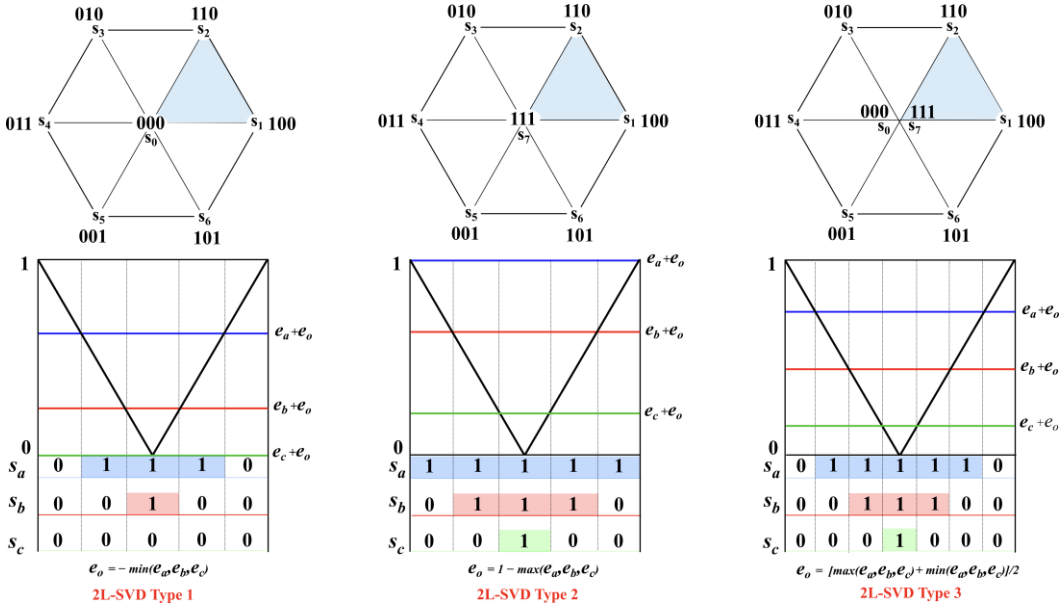

Fig. 5. Two-level PWM implementation

which are compared against carrier waveforms to generate the corresponding two-level switching pulses. Finally, the switching states of the 4L-NNPC inverter are synthesized using these modulating signals together with the selected base states.

Table 2. Region identification rule

2L-SVD Type	Condition		$\vec{\mathbf{L}}$
1	*mid – min > 2*	*min* = v_{cs}	$\overrightarrow{220}$
		min = v_{as}	$\overrightarrow{022}$
		min = v_{bs}	$\overrightarrow{202}$
2	*max – mid > 2*	*max* = v_{as}	$\overrightarrow{200}$
		max = v_{bs}	$\overrightarrow{020}$
		max = v_{cs}	$\overrightarrow{002}$
3	*max – min < 1*	-	$\overrightarrow{111}$
	max – min > 1	$v_{as} > v_{bs} > v_{cs}$	$\overrightarrow{210}$
		$v_{bs} > v_{as} > v_{cs}$	$\overrightarrow{120}$
		$v_{bs} > v_{cs} > v_{as}$	$\overrightarrow{021}$
		$v_{cs} > v_{bs} > v_{as}$	$\overrightarrow{012}$
		$v_{cs} > v_{as} > v_{bs}$	$\overrightarrow{102}$
		$v_{as} > v_{cs} > v_{bs}$	$\overrightarrow{201}$

3.2. Voltage Balancing Control of Flying Capacitors

This section explains how appropriate redundant switching states can be chosen for generating intermediate voltage levels. As listed in Table 1, two redundant state pairs (1a, 1b) and (2a, 2b)-are available for these levels. The choice among these states should contribute to maintaining the voltage balance of the flying capacitors (FCs).

Assume the difference between the FC voltage and it's rated value is defined as:

$$\Delta_{C_{k,x}}(t) = v_{C_{k,x}}(t) - V_d/3 \qquad (16)$$

where $x = \{a, b, c\}$, and $k = \{1, 2\}$. The principle of proposed voltage balancing control is to prioritize balancing the capacitor with the largest voltage deviation. At each control interval, the absolute voltage deviations $\left|\Delta_{C_{k,x}}(t)\right|$ of the two flying capacitors are compared, and the capacitor exhibiting the largest deviation is selected for the balancing action. A variable ρ_x is defined to determine which capacitor has the larger deviation and therefore requires higher balancing priority:

$$\rho_x = max\left\{\left|\Delta_{C_{1,x}}(t)\right|, \left|\Delta_{C_{2,x}}(t)\right|\right\} \qquad (17)$$

Once the target capacitor is identified, the control algorithm evaluates the capacitor function f_{Cix}, which is the product of the capacitor voltage deviation and the phase current as:

$$f_{Cix} = \begin{cases} \Delta_{C_{1,x}}(t) \times i_x(t) & if\ \ \rho_x = \left|\Delta_{C_{1,x}}(t)\right| \\ \Delta_{C_{2,x}}(t) \times i_x(t) & if\ \ \rho_x = \left|\Delta_{C_{2,x}}(t)\right| \end{cases} \qquad (18)$$

The sign of this function determines whether the capacitor is currently charging or discharging. Then, the algorithm selects an appropriate redundant state to balance capacitor voltage as in Table 3. For example, assume that $S_x = 2$, and C_{1x} has priority over C_{2x}. In this case, $f_{Cix} = \Delta_{C_{1,x}}(t) \times i_x(t) \geq 0$, a switching state must be selected in which, C_{1x} is discharged. Hence, the switching state 2b is selected. Similarly, if $f_{Cix} < 0$, a redundant switching state must be selected where C_{1x} is charged, and switching state 2a is selected. Combine the carrier-based PWM with the VBC algorithm, flow chart of the proposed scheme is presented in Fig. 6.

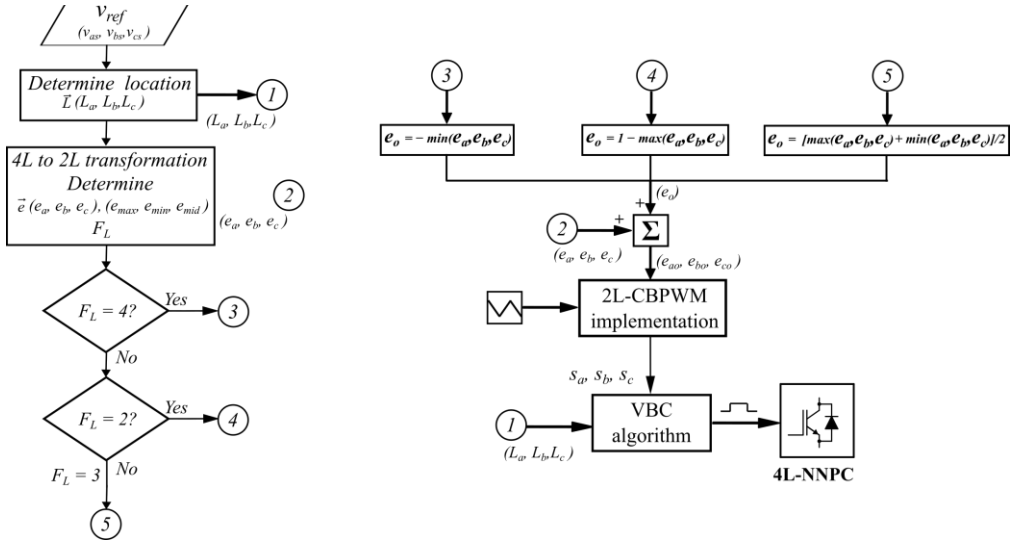

Fig. 6. Flow chart of the proposed scheme

Table 3. Logic table of voltage balancing control

S_x	Condition	State
1	$f_{Cix} \geq 0$	1b
	$f_{Cix} < 0$	1a
2	$f_{Cix} \geq 0$	2b
	$f_{Cix} < 0$	2a

4. SIMULATION RESULTS

The operating performance of the proposed 4L-NNPC motor drive is evaluated using both the conventional SPWM method and the modified carrier-based PWM strategy under various operating conditions. For all simulations, the dc-link voltage of the 4L-NNPC inverter is set to 7000 V. Each flying capacitor is rated at 2333 V and designed with a capacitance value of 2200 μF. The carrier waveforms are triangular signals generated at 5 kHz. The indirect field-oriented control (IFOC) is implemented with a reference rotor flux magnitude of 8.35 Wb and a rated rotor speed of 1189 rpm. The remaining system parameters are summarized in Table 4.

Table 4. Simulation parameters

Parameter	Value
Motor rated power	1250 hp
Pole pairs	3
Rated voltage	4160 V
Rated speed	1189 rpm
Rated torque	7490 Nm
Stator resistance	0.21 Ω
Rotor resistance	0.146 Ω
Stator leakage inductance	5.2 mH
Rotor leakage inductance	5.2 mH

Parameter	Value
Magnetizing inductance	155 mH
Moment of inertia	22 kg.m
Switching frequency	5 kHz

4.1. Steady-state performance

Fig.7(a) illustrates the rated-speed operation of the 4L-NNPC motor drive system employing the conventional IPD-PWM scheme under rated conditions, whereas Fig. 7(b) corresponds to the operation with the proposed scheme. In both cases, the rotor speed (N) is accurately regulated at its reference value (N^*) of 1189 rpm by the speed controller. Simultaneously, the motor develops an electromagnetic torque Te of approximately 7490 Nm to satisfy the load torque (T_m) requirement. Nevertheless, noticeable torque ripples are observed with the IPD-PWM scheme. In particular, the peak-to-peak electromagnetic torque ripple reaches 462 Nm for the IPD-PWM method, whereas it is reduced to 340 Nm when the proposed scheme is applied. This improvement is mainly attributed to the enhanced voltage waveform quality achieved by the proposed PWM, which provides a more uniform switching distribution and reduces low-order harmonic components affecting the torque.

Regarding output quality, the line-to-line voltage THD and stator current THD obtained with IPD-PWM are 24.5% and 1.81%, respectively. In contrast, the proposed scheme achieves lower THDs of 24.2% for the line voltage and 1.22% for the stator current. The reduction in current THD is more pronounced due to the filtering effect of the motor inductance, while the improved voltage waveform results from more effective utilization of redundant switching states in the proposed modulation scheme.

It is observed that both schemes maintain low FC's voltage ripples, approximately 2% of the rated capacitor voltage. This indicates that the capacitor voltage balancing mechanism operates effectively in both cases under rated conditions. However, the proposed method significantly reduces the common-mode voltage (CMV). Specifically, the peak-to-peak CMV is limited to 1178 V, compared to 1975 V under the conventional IPD-PWM scheme. This reduction is achieved by selecting switching states that constrain the CMV level, thereby limiting the CMV amplitude.

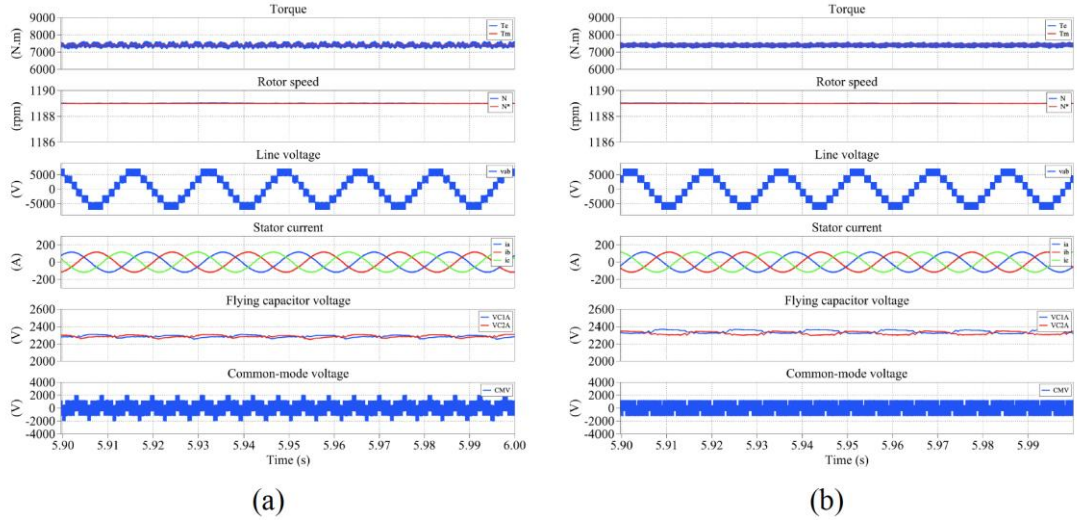

Fig. 7. Steady-state waveforms under rated-speed operation with (a) Conventional IPDPWM, (b) The proposed scheme

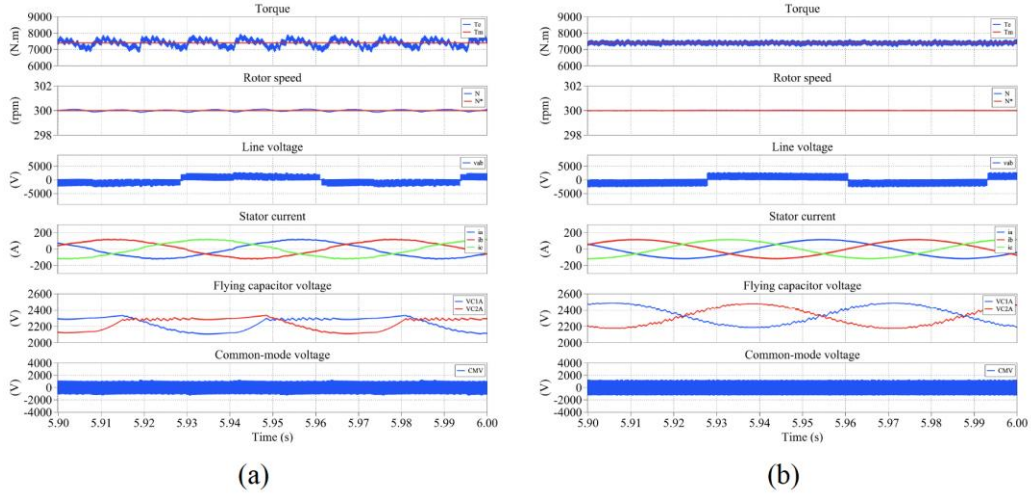

Fig. 8. Steady-state waveforms under low-speed operation with
(a) Conventional IPDPWM, (b) The proposed scheme

Fig. 8 presents a comparison of the low-speed performance of the system under the conventional IPD-PWM and the proposed scheme. Although both schemes successfully regulate the rotor speed at 300 rpm and meet the load torque requirement, the IPD-PWM results in pronounced torque oscillations with a peak-to-peak ripple of 1112 Nm, whereas this value is significantly reduced to 470 Nm with the proposed approach. Moreover, the proposed scheme reduces the stator current THD from 5.09% to 2.40%. Although the proposed method slightly increases the FC's voltage ripple from 10.2% to 12.9%, it effectively maintains the average capacitor voltage close to its reference value. In contrast, the IPD-PWM leads to a noticeable reduction of the capacitor voltage below the rated value.

4.2. Dynamic simulation

Fig. 9 illustrates the dynamic performance of the proposed scheme. At t = 5 s, a step increase in the load torque from 0 to 7490 Nm is applied while the rotor speed is maintained at its rated value of 1189 rpm. After the load change, the actual rotor speed remains well regulated, exhibiting only a brief transient response. Under no-load conditions, the developed electromagnetic torque is approximately zero.

At the step time, the electromagnetic torque rapidly tracks the reference with only a slight overshoot. During this transient, the 4L-NNPC maintains stable line-to-line voltages that are unaffected by the load torque variation. In contrast, the stator current magnitude increases with the torque demand. In addition, the floating capacitor voltages are regulated around 2333 V, with ripple amplitudes increasing proportionally to the load current. Overall, these results confirm that the proposed control strategy satisfies both the FOC control requirements and the output waveform objectives of the 4L-NNPC under dynamic operating conditions.

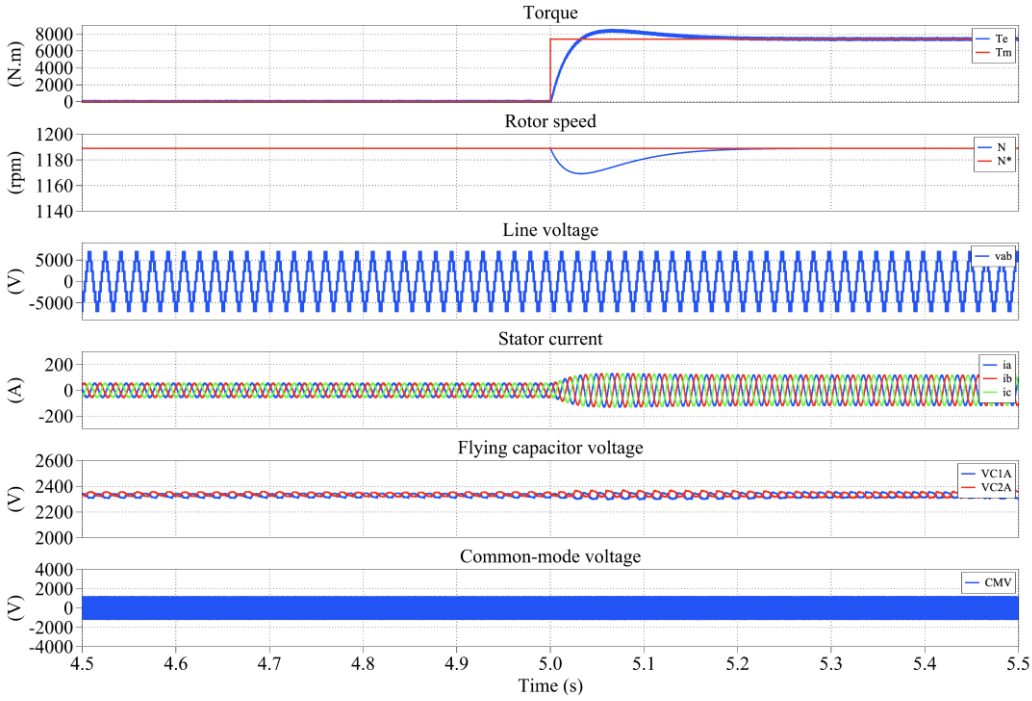

Fig. 9. Dynamic performance of the proposed scheme

5. CONCLUSION

This paper proposes a high-performance control strategy for a field-oriented controlled medium-voltage induction motor drive fed by a four-level neutral-point clamped inverter. The proposed approach integrates a modified carrier-based PWM scheme with an effective flying capacitor voltage balancing mechanism to simultaneously improve output waveform quality and mitigate common-mode voltage. The effectiveness of the proposed strategy has been validated under steady-state, low-speed, and dynamic operating conditions. Simulation results demonstrate that the proposed method significantly enhances the overall drive performance compared with the conventional IPD-PWM scheme. In particular, the stator current THD is noticeably reduced, while the electromagnetic torque ripple is substantially suppressed, leading to smoother torque production and reduced mechanical stress on the motor shaft. Although a moderate increase in floating capacitor voltage ripple is observed in certain operating conditions, the proposed strategy successfully maintains the average capacitor voltages close to their reference values, thereby ensuring stable inverter operation and long-term reliability. Moreover, a considerable reduction in peak-to-peak common-mode voltage is achieved, which effectively alleviates insulation stress and bearing-related issues in medium-voltage motor drives. Overall, the proposed control strategy satisfies both motor control objectives and inverter-side performance requirements, offering a robust for medium voltage drive applications. The improved THD, reduced CMV, and enhanced voltage balancing capability make the proposed approach well suited for high-performance and industrial drive systems.

REFERENCES

[1] B. Wu and M. Narimani, *High-power converters and AC drives*, 2nd ed. Wiley-IEEE Press, Jan 2017.

[2] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: Challenges and existing technology," *IEEE Power Electronics Magazine*, vol. 3, no. 2, pp. 29-41, June 2016, doi: https://doi.org/10.1109/MPEL.2016.2551802.

[3] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE Ind. Appl. Mag.*, vol. 18, no. 4, pp. 26–39, Jul 2012, doi: https://doi.org/10.1109/MIAS.2012.2192231.

[4] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, ''Multilevel voltage-source-converter topologies for industrial medium-voltage drives,'' *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007, doi: https://doi.org/10.1109/TIE.2007.907044.

[5] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. P.rez, and Author image of Jose I. Leon J. I. Leon, ''Recent advances and industrial applications of multilevel converters,'' *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010, doi: https://doi.org/10.1109/TIE.2010.2049719.

[6] J. Pou, R. Pindado, and D. Boroyevich, ''Voltage-balance limits in four-level diodeclamped converters with passive front ends,'' *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005, doi: https://doi.org/10.1109/TIE.2004.837915.

[7] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec. 2014, doi: https://doi.org/10.1109/TPEL.2014.2306191.

[8] K. Tian, B. Wu, M. Narimani, D. D. Xu, Z. Cheng, and N. R. Zargari, "A capacitor voltage-balancing method for nested neutral point clamped (NNPC) inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2575–2583, Mar. 2016, doi: https://doi.org/10.1109/TPEL.2015.2438779.

[9] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A novel and simple single-phase modulator for the nested neutral-point clamped (NNPC) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4069–4078, Aug. 2015, doi: https://doi.org/10.1109/TPEL.2014.2352649.

[10] L. Tan et al. "A space virtual-vector modulation with voltage balance control (VBC) for nested neutral-point clamped converter under low output frequency conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3458–3466, May 2017, doi: https://doi.org/10.1109/TPEL.2016.2589941.

[11] L. Tan et al., "A simplified space vector modulation for four-level nested neutral point clamped inverters with complete control of flying-capacitor voltages," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1997–2006, Mar. 2018, doi: https://doi.org/10.1109/TPEL.2017.2697847.

[12] K. Tian, B. Wu, M. Narimani, D. Xu, Z. Cheng, and N. R. Zargari, "A space vector modulation method for common-mode voltage reduction in nested neutral point clamped inverter," *Proc. IEEE 40th Annu. Conf. Ind. Electron. Soc.*, 2014, pp. 4541–4547, doi: https://doi.org/10.1109/IECON.2014.7049187.

[13] L. N. Pham, K. D. Pham, Q. D. Phan, and N. -V. Nguyen, "Novel Virtual Vector SVPWM Method to Mitigate Low-Frequency Common Mode Voltage for Four-Level

NPC Inverters," *IEEE Access*, vol. 12, pp. 22403-22419, 2024, doi: https://doi.org/10.1109/ACCESS.2024.3362789.

[14] L. N. Pham, Q. D. Phan, and N. -V. Nguyen, "Simplified Carrier-Based SVDPWM Methods Using Reduced Common Mode Voltage Vector Redundancy for Improving Output Current Ripple in Four-Level NPC Inverter," *IEEE Access*, vol. 13, pp. 124962-124978, 2025, https://doi.org/10.1109/ACCESS.2025.3589572.

[15] L. N. Pham, Q. D. Phan, and V. N. Nguyen, "Current-Based SVDPWM with Reduced Common-Mode Voltage for Switching Loss Minimization in Four-Level NPC Inverters," *J. Electr. Eng. Technol.*, vol. 21, no. 3, pp. 2713–2731, 2026, doi: https://doi.org/10.1007/s42835-026-02587-1.

[16] H. Le, A. Dekka, and D. Ronanki, "Low-Speed Operation of a New Four-Level Multilevel Inverter fed Medium-Voltage Drive," *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, 2022, pp. 1-6, doi: https://doi.org/10.1109/PEDES56012.2022.10080642.