DOI: https://doi.org/10.62985/j.huit_ojs.vol26.no2E.382

A SIMPLIFIED SVPWM METHOD TO REDUCE COMMON-MODE VOLTAGE FOR VOLTAGE SOURCE INVERTER

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Received: 12 September 2025; Revised: 8 March 2026; Accepted: 18 April 2026

ABSTRACT

This study introduces a hybrid space vector pulse width modulation strategy aimed at mitigating common-mode voltage (CMV) in voltage source inverters. The proposed approach integrates the characteristics of Near-State PWM (NSPWM) and Active Zero-State PWM (AZSPWM) within a unified modulation framework. The space-vector diagram is partitioned into four operating regions, where only active voltage vectors are utilized for modulation. To enable practical implementation, a simplified carrier-based realization is developed using two triangular carriers with a 180° phase displacement. An offset formulation is derived for each operating region of the reference vector to generate the required switching signals. Compared with the conventional 120° phase-shifted carrier PWM technique, the proposed scheme significantly suppresses CMV across the entire space-vector plane. In addition, incorporating the NSPWM concept reduces switching transitions, leading to lower switching power losses and improved overall efficiency. The effectiveness of the modulation strategy is verified through simulation studies conducted in MATLAB/Simulink and PLECS. The results confirm that the proposed technique achieves effective CMV suppression while maintaining a simple implementation structure, making it suitable for digital control platforms with limited computational resources.

Keywords: Space-vector PWM, Carrier-based PWM, Common-mode voltage suppression, Voltage-source inverter.

1. INTRODUCTION

Three-phase voltage source inverters (VSIs) play an essential role in a wide range of power electronic applications, including motor drive systems, grid-connected photovoltaic converters, and uninterruptible power supplies (UPSs) (Fig. 1) [1], [2]. Because of their relatively simple topology, high conversion efficiency, and versatile control capability, VSIs have become one of the most widely used solutions for DC–AC energy conversion. Despite these advantages, the switching actions of two-level VSIs inherently produce common-mode voltage (CMV), which can lead to several undesirable effects in practical systems.

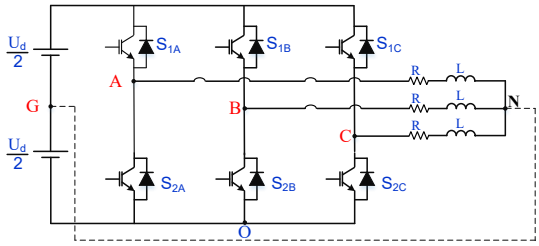


Fig. 1. Voltage Source Inverter Topology

Excessive CMV is well known to cause various undesirable effects, including high-frequency common-mode voltages, bearing corrosion in electrical machine applications, increased leakage currents in transformerless loads, and elevated electromagnetic interference (EMI). These issues necessitate advanced PWM techniques capable of mitigating CMV while maintaining the voltage quality at the inverter output [3], [4].

These limitations motivate the development of modulation techniques capable of suppressing CMV while preserving output voltage quality and avoiding additional switching losses. To address this issue, a variety of CMV mitigation strategies derived from space vector pulse width modulation (SVPWM) have been investigated in the literature. Representative methods include equal-CMV SVPWM, active zero-vector modulation, near-state PWM, and remote-state PWM (Fig. 2) [5] - [8]. Despite their effectiveness, many space-vector-based solutions rely on relatively complicated computational procedures, which may hinder their implementation in real-time digital control platforms [9]-[11].

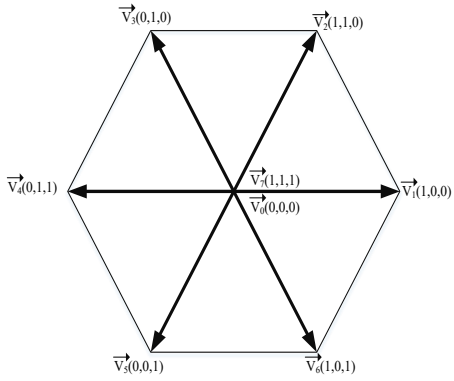


Fig. 2. Space vector diagram of 2L-voltage Source Inverter

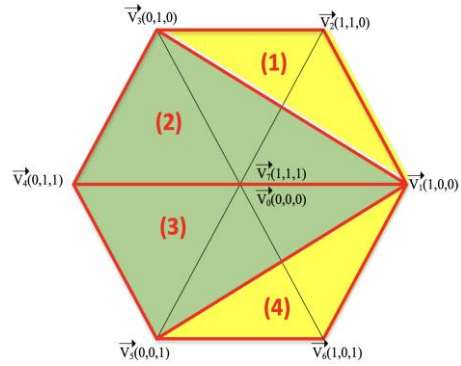


Fig. 3. Space vector division of the proposed reduced CMV SVPWM method

In contrast, carrier-based PWM (CBPWM) offers a simpler modulation structure; however, only a limited number of CBPWM methods have been proposed for CMV reduction. A representative approach is the phase-shifted CBPWM scheme employing three carriers shifted by 120° [12]. Nevertheless, a major drawback of this method is its inability to effectively reduce common-mode voltage. Over the entire space vector diagram, relatively high CMV amplitudes still appear in many operating regions of the reference vector.

To overcome this limitation, this paper introduces a new, simple carrier-based SVPWM implementation that is capable of reducing CMV over the entire space vector diagram (Fig. 3).

Compared with conventional NSPWM-based methods, the proposed hybrid SVPWM strategy preserves the reduced switching transition characteristic by clamping one phase within each operating region, thereby contributing to lower switching power losses. In contrast to AZSPWM-based approaches, which mainly focus on common-mode voltage suppression through active zero-state synthesis, the proposed method further simplifies the implementation by using only two fixed triangular carriers with a 180° phase shift and a region-dependent offset function. As a result, the proposed scheme combines the low-switching-loss benefit of NSPWM and the CMV-reduction capability of AZSPWM within a unified carrier-based framework. In addition, the proposed strategy achieves CMV suppression over the entire space-vector plane while maintaining a simple control structure suitable for low-cost digital controllers.

2. THE PROPOSED HYBRID SVPWM METHOD

2.1. Common-Mode Voltage

In a conventional two-level voltage source inverter, the common-mode voltage (CMV) represents the average value of the three phase terminal voltages referenced to the DC-link midpoint. Accordingly, CMV can be expressed as:

$$V_{com} = V_{NG} = \frac{V_{AG}+V_{BG}+V_{BG}}{3} \quad (1)$$

V_{AG}, V_{BG}, V_{CG} are output inverter voltage of A-B- and C-phases:

$$\begin{cases} V_{AG} = V_{AO} - \frac{U_d}{2} \\ V_{BG} = V_{BO} - \frac{U_d}{2} \\ V_{CG} = V_{CO} - \frac{U_d}{2} \end{cases} \quad (2)$$

By replacing (1) into (2), we obtain:

$$V_{com} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} - \frac{V_d}{2} \quad (3)$$

The switching states of the three inverter legs are represented by SA, SB, and SC . Based on these variables, (3) can be rewritten as:

$$V_{com} = \left(\frac{S_A+S_B+S_C}{3} - \frac{1}{2}\right) U_d \quad (4)$$

According to (4), the CMV switching states are summarized in Table 1.

Table 1. Common-mode voltage magnitude in a two-level VSI

Vectors	Switching states	Common mode voltages
Zero vectors	$\overrightarrow{v_0}(0,0,0)$	$-\mathrm{U_d}/2$
	$\overrightarrow{v_7}(1,1,1)$	$\mathrm{U_d}/2$
Nonzero- vectors	$\overrightarrow{v_1}(1,0,0)$, $\overrightarrow{v_3}(0,1,0)$, $\overrightarrow{v_5}(0,0,1)$	$-\mathrm{U_d}/6$
	$\overrightarrow{v_2}(1,1,0)$, $\overrightarrow{v_4}(0,1,1)$, $\overrightarrow{v_6}(1,0,1)$	$\mathrm{U_d}/6$

The two zero vectors [000] and [111] generate the maximum CMV and are therefore eliminated in CMV-reduction PWM techniques.

2.2. Principle of the Proposed SVPWM

Fig. 3 illustrates the modulation concept of the proposed SVPWM strategy. The space-vector plane is divided into four distinct sectors, denoted as Regions 1–4.

Within each region, the desired reference vector Vref is constructed using a sequence of three active switching vectors V1, V2, and V3 . Their respective application durations, defined as T1, T2, and T3, are determined according to the SVPWM relationship described in (5).

$$\begin{cases} V_{ref}T_S = V_1.T_1 + V_2.T_2 + V_3.T_3 \\ T_S = T_1 + T_2 + T_3 \end{cases} \quad (5)$$

Here T_S denotes the sampling period. Specifically, the vector sequence in each region is implemented as follows:

Region 1: 100 → 110 → 010

Region 2: $100 \rightarrow 010 \rightarrow 011$

Region 3: $100 \rightarrow 001 \rightarrow 011$

Region 4: $100 \rightarrow 101 \rightarrow 001$

1) Determination of Regions

Based on the control region partition shown in Fig. 3, the boundaries of Regions 1, 2, 3, and 4 are determined as summarized in Table 2.

Table 2. Determination of Regions

Region	Determination of Regions
1	$v_c < -1/3$
2	$v_c > -1/3$ & $v_b - v_c > 0$
3	$v_b > -1/3$ & $v_c - v_b > 0$
4	$v_b < -1/3$

2) Calculation of the Dwell Times:

We consider a load voltage vector $\overline{V}_t = V_m e^{j\theta}$, where V_m, and θ denote the voltage magnitude and phase angle, respectively.

The three-phase load voltages may alternatively be represented using V_A, V_B, V_C as:

$$\begin{cases} V_A = V_m.cos\theta \\ V_B = V_m.\cos(\theta - \frac{2\pi}{3}) \\ V_C = V_m.\cos(\theta - \frac{4\pi}{3}) \end{cases} \quad (6)$$

Let v_a, v_b, v_c, v_o denote the normalized voltages of the phase voltages V_A, V_B, V_C and the offset voltage, respectively:

$$v_a = \frac{V_A}{V_d}, v_b = \frac{V_B}{V_d}; v_c = \frac{V_C}{V_d}; v_o = \frac{V_O}{V_d}$$

In the proposed SVPWM scheme, the reference vector may lie in different regions of the space-vector diagram, and the dwell times are determined by the switching sequence employed in each region. Region 1 is considered, from the sequence diagram in Table 2, phase C is clamped at zero. Consequently, the offset voltage can be derived as -vc:

$S_c = 0 \quad \Rightarrow v_c + v_o = 0 \quad \Rightarrow v_o = -v_c$

Accordingly, the high-level (logic "1") duty ratios of phases A, B, and C, denoted by D_a, D_b, D_c. are obtained as follows:

$D_a = v_a + v_o = v_a - v_c$

$D_b = v_b + v_o = v_b - v_c$

$D_c = 0$

Based on these duty ratios, the dwell times of the active voltage vectors can be determined as:

$T_{100} = (1-D_b)T_S = (1-v_b+v_c)T_S$

$T_{010} = (1-D_a)T_S = (1-v_a+v_c)T_S$

$T_{110} = T_S - T_{100} - T_{010}$

In the remaining regions, the corresponding durations of the active voltage vectors can be determined in a similar manner, as summarized in Table 3 below.

Table 3. Dwell time calculation

Region	PWM	The dwell times
1	$D_a.T_S$ T_{010} 1 1 0 SA 0 1 1 SB 0 0 0 SC T_{100} $D_b.T_S$	$T_{100}=(1-D_b)T_S=(1-v_b+v_c)T_S$ $T_{010}=(1-D_a)T_S=(1-v_a+v_c)T_S$ $T_{110}= T_S-T_{100}-T_{010}$
2	T_{100} 1 0 0 SA 0 1 1 SB 0 0 1 SC T_{011}	$T_{100}=D_a.T_S=\left(v_a+\frac{1-v_a-v_b}{2}\right)T_S$ $T_{011}=D_c.T_S=\left(v_c+\frac{1-v_a-v_b}{2}\right)T_S$ $T_{010}= T_S-T_{100}-T_{011}$
3	T_{100} T_{011} 1 0 0 SA 0 0 1 SB 0 1 1 SC	$T_{100}=D_a.T_S=\left(v_a+\frac{1-v_a-v_c}{2}\right)T_S$ $T_{011}=D_b.T_S=\left(v_b+\frac{1-v_a-v_c}{2}\right)T_S$ $T_{001}= T_S-T_{100}-T_{011}$
4	$D_a.T_s$ T_{001} 1 1 0 SA 0 0 0 SB 0 1 1 SC T_{100} $Dc.T_s$	$T_{100}=(1-D_c)T_S=(1-v_c+v_b)T_S$ $T_{001}=(1-D_a)T_S=(1-v_a+v_b)T_S$ $T_{101}= T_S-T_{100}-T_{001}$

With the region boundaries determined in Table 2 and the corresponding dwell times given in Table 3, the proposed SVPWM technique can be implemented.

3. CARRIER IMPLEMENTATION OF THE PROPOSED SVPWM

The SVPWM algorithm described above can be further simplified by replacing it with a carrier-based PWM technique through the determination of the control voltages $v_{đkA}$,$v_{đkB}$, and $v_{đkC}$. The flowchart of this carrier-based PWM algorithm is illustrated in Fig. 4. To compute these control signals, the offset voltage in each region (Regions 1, 2, 3, and 4) must be determined.

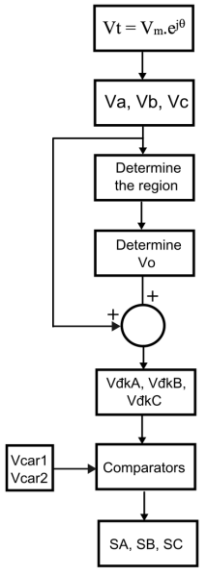


Fig. 4. Algorithm of the proposed hybrid SVPWM technique

Based on the average voltage model of the three-phase inverter illustrated in Fig. 5, we have:

$$\begin{cases} V_{AO} = V_A + V_O \\ V_{BO} = V_B + V_O \\ V_{CO} = V_C + V_O \end{cases} \quad (7)$$

When using a triangular carrier in the range (0,1) and expressing the variables in normalized form, we obtain :

$$\Rightarrow \begin{cases} V_{đkA} = v_a + v_o = D_A \\ V_{đkB} = v_b + v_o = D_B \\ V_{đkC} = v_c + v_o = D_C \end{cases} \quad (8)$$

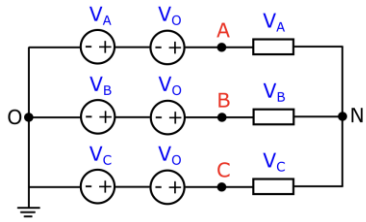


Fig. 5. Voltage Source Inverter Modeling

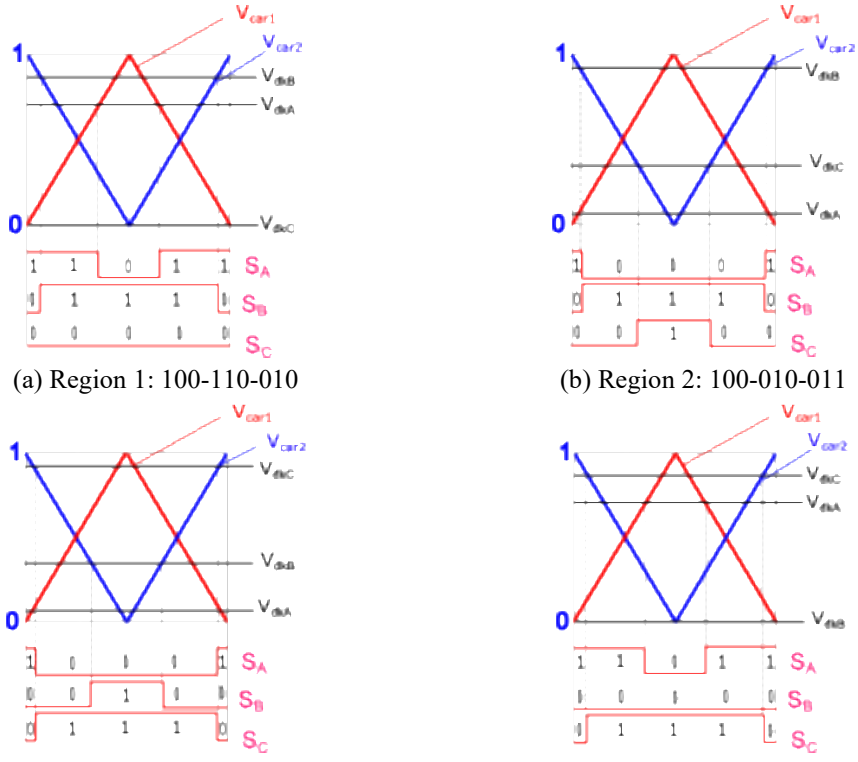
The offset v_o for Regions 1, 2, 3, and 4 in (8), derived in Section 2.2, is summarized in Table 4.

Table 4. Determination of V_O

Region	PWM	Conditions	$\mathbf{v_O}$
1	1 1 0 SA 0 1 1 SB 0 0 0 SC	$v_c+v_o = 0$	$v_O = -v_c$
2	1 0 0 SA 0 1 1 SB 0 0 1 SC	Da + Db=1	$v_O = \frac{1 - v_a - v_b}{2}$
3	1 0 0 SA 0 0 1 SB 0 1 1 SC	Da + Dc=1	$v_O = \frac{1 - v_a - v_c}{2}$
4	1 1 0 SA 0 0 0 SB 0 1 1 SC	$v_b+v_o = 0$	$v_O = -v_b$

The design phase opposite carrier waveforms:

The proposed method employs two triangular carriers with a 180° phase shift. The carrier Vcar1 is used for phase A, while the carrier Vcar2 is applied to both phases B and C. The three-phase control signals A, B, and C are compared with their respective carrier signals to generate the gating pulse sequences shown in Figs. 6(a)–6(d). These figures illustrate the switching state sequences when the reference voltage vector lies in Regions 1–4 of the space-vector diagram.



(a) Region 1: 100-110-010 (b) Region 2: 100-010-011

(c) Region 3: 100-001-011 (d) Region 4: 100-101-001

Fig. 6. Switching-state sequences and carrier comparison principle of the proposed method in the four regions

4. SIMULATION RESULTS

A simulation model of a two-level three-phase inverter with an RL load is developed in MATLAB. The main simulation parameters are presented in Table 5.

Table 5. Simulation parameters of the three-phase inverter

Parameter	Symbol	Value	Unit
DC source voltage	Vd	600	V
Output fundamental frequency	f	50	Hz
Switching frequency	f_{sw}	5	kHz
Load resistance	R	10	Ω
Load inductance	L	10	mH

Fig. 7 shows the waveforms of the three-phase control voltages V_{dkA}, V_{dkB}, and V_{dkC} and the corresponding offset voltage v_o when the modulation index is m = 0.2 and m = 0.8

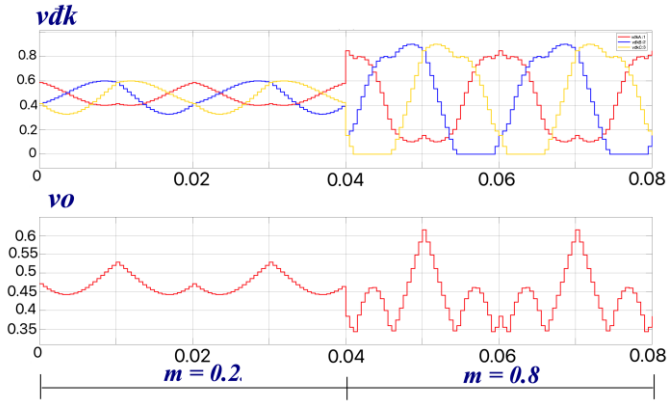
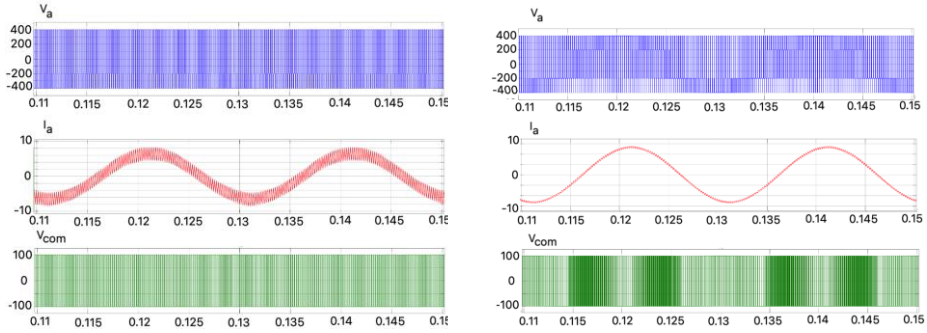


Fig. 7. Waveforms of the three-phase modulating signals đkA, vđkB, vđkC and offset v_o when m = 0.2 (t < 0.04) and m = 0.8 (t > 0.04)

Figs. 8(a) and 8(b) present the simulated waveforms of the phase voltage v_a, load current i_a, and common-mode voltage v_{com} obtained using the proposed SVPWM method at modulation indices m = 0.2 and m = 0.8, respectively. When m = 0.2, the total harmonic distortions of the voltage and current are THD_u = 772.83% and THD_i = 23.88%, respectively. As the modulation index increases to m=0.8, these values decrease to THD_u = 125.93% and THD_i = 3.42%. The results indicate that the harmonic distortion decreases as the modulation index increases.



(a) m = 0.2 (b) m=0.8

Fig. 8. Diagrams of the phase voltage, load current, and CMV by the proposed SVPWM method for: a) m = 0.2; b) m = 0.8

When m=0.2, the reference vector lies in Regions 2 and 3. Considering phase-A voltage as an example, it switches among the levels 400 V, −200 V, and −400 V in Regions 2 and 3.

For m=0.8, the reference voltage vector traverses all four regions (Regions 1, 2, 3, and 4). In this case, the phase-A voltage varies among 400 V, 200 V, and −200 V in Region 1; among 400 V, −200 V, and −400 V in Region 2; among 400 V, −200 V, and −400 V in Region 3; and among 400 V, 200 V, and −200 V in Region 4.

The CMV peak observed in both cases is limited to ±100 V (±Vd/6).

Compared with the phase-shifted PWM (PS-PWM) method, the proposed approach operates over an extended modulation index range up to m=1. In this case, the three-phase control voltages $V_{đkA}$, $V_{đkB}$, and $V_{đkC}$ and the offset v_o are illustrated in Fig. 9. The phase A voltage attains the levels 400 V, −200 V, and −400 V, while the CMV is limited to ±100V (±Vd/6), as shown in Fig. 10. The output voltage and current quality are further improved, with harmonic distortion levels of THDu=63.22% and THDi=1.59%.

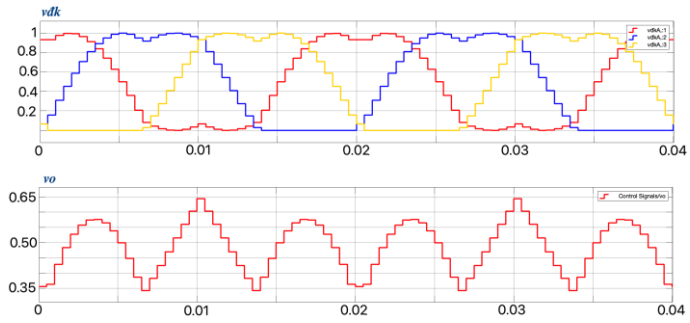


Fig. 9. Waveforms of the three-phase modulating signals vđkA, vđkB, vđkC, and offset v_o for m = 1

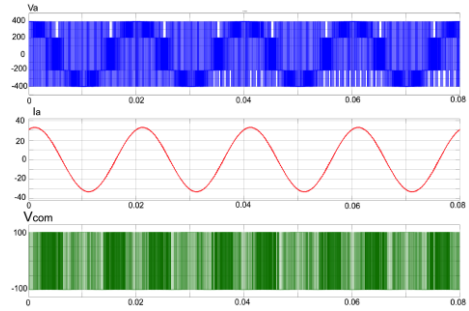
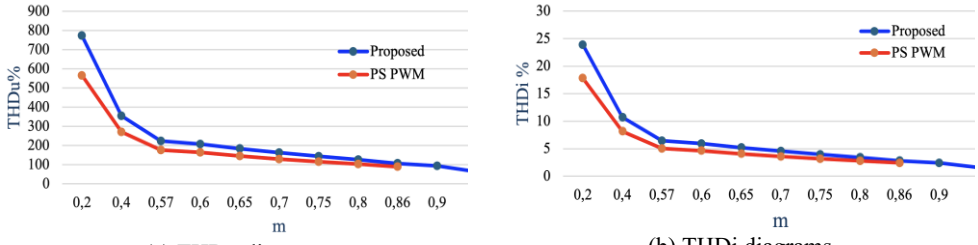


Fig. 10. Diagrams of the load voltage, load current, and CMV by the proposed SVPWM method for m = 1

The voltage and current harmonic distortion characteristics, THDu and THDi, of the proposed SVPWM method are extensively investigated over the full modulation index range and presented in Fig. 11.



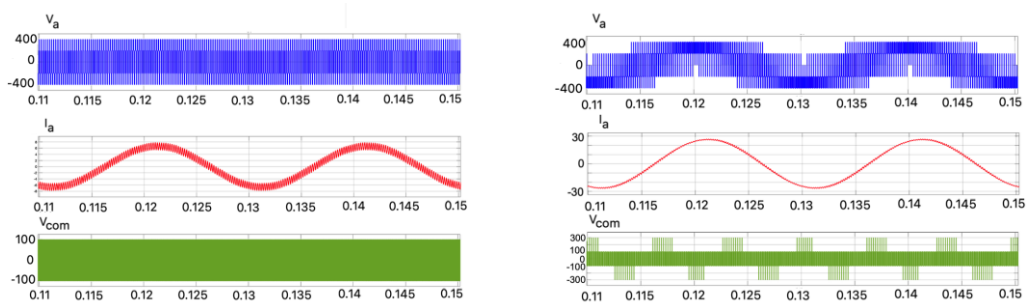
(a) THDu diagram

(b) THDi diagrams

Fig. 11. The output voltage and current THD diagrams: a) THDU; b) THDI

For comparison purposes, the load voltage, load current, and CMV waveforms obtained with the PS-PWM strategy are also presented in Fig. 9. When the modulation index is m=0.2, the CMV magnitude is limited to approximately ±100 V (±Vd/6). As the modulation index increases to m=0.8, the CMV rises to around ±300 V (±Vd/2). This indicates that the PS-PWM approach is unable to maintain CMV suppression across the entire modulation range.

The THD characteristics of the output voltage and current obtained using the PS-PWM method are further presented in Fig. 12. The results indicate that the improvement in output waveform quality is relatively limited.



(a) m = 0.2 (b) m=0.8

Fig. 12. Waveforms of the load voltage and current, and CMV using the PS- PWM technique for a) m = 0.2; b) m = 0.8

PLECS is employed to evaluate the switching power losses and to perform a comparison between the proposed modulation strategy and the PS-PWM method. The obtained results indicate that the proposed approach yields lower switching losses, as illustrated in Fig. 13.

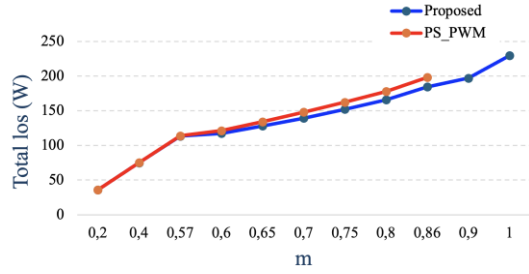


Fig. 13. Comparison of total loss between PS-PWM and the proposed method

5. CONCLUSION

This study presents a hybrid space-vector pulse width modulation (SVPWM) strategy designed to mitigate common-mode voltage (CMV) in voltage source inverters. The proposed modulation strategy divides the space-vector diagram into four operating regions and reconstructs the reference vector using only active voltage vectors. To implement this hybrid SVPWM scheme, a new and simple carrier-based algorithm is designed, which utilizes only two fixed triangular carriers with a 180° phase shift. In addition, appropriate offset functions are derived for each operating region of the reference vector.

Results obtained from MATLAB/Simulink and PLECS simulations confirm that the proposed modulation strategy effectively suppresses CMV over the entire space-vector plane while simultaneously reducing switching losses. Consequently, higher overall efficiency is achieved compared with the conventional PS-PWM approach. Owing to its simple carrier-based implementation, the proposed algorithm is well suited for cost-effective embedded microcontroller platforms.

Acknowledgment: We acknowledge Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for supporting this study.

REFERENCES

[1] H. Chen and H. Zhao, 'Review on pulse-width modulation strategies for common-mode voltage reduction in three-phase voltage-source inverters', Nov. 16, 2016, *Institution of Engineering and Technology*. doi: https://doi.org/10.1049/iet-pel.2015.1019.

[2] E. Robles, M. Fernandez, J. Andreu, E. Ibarra, and U. Ugalde, 'Advanced power inverter topologies and modulation techniques for common-mode voltage elimination in electric motor drive systems', Apr. 01, 2021, *Elsevier Ltd.* doi: https://doi.org/10.1016/j.rser.2021.110746.

[3] Y. Huang *et al.*, 'Analytical characterization of CM and DM performance of three-phase voltage-source inverters under various PWM patterns', *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4091–4104, 2021, doi: https://doi.org/10.1109/TPEL.2020.3024836.

[4] H. Qamar, H. Qamar, and R. Ayyanar, 'Performance Analysis and Experimental Validation of 240°-Clamped Space Vector PWM to Minimize Common Mode Voltage and Leakage Current in EV/HEV Traction Drives', *IEEE Trans. Transp. Electrif.*, vol. 8, no. 1, pp. 196–208, 2022, doi: https://doi.org/10.1109/TTE.2021.3108957.

[5] A. M. Hava and E. Ün, 'Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters', *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, 2009, doi: https://doi.org/10.1109/TPEL.2008.2005719.

[6] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, 'Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters', *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013, doi: https://doi.org/10.1109/TPEL.2012.2196712.

[7] S. K. Mun and S. Kwak, 'Reducing common-mode voltage of three-phase VSIs using the predictive current control method based on reference voltage', *J. Power Electron.*, vol. 15, no. 3, pp. 712–720, Jan. 2015, doi: https://doi.org/10.6113/JPE.2015.15.3.712.

[8] A. Janabi and B. Wang, 'Hybrid SVPWM Scheme to Minimize the Common-Mode Voltage Frequency and Amplitude in Voltage Source Inverter Drives', *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1595–1610, Feb. 2019, doi: https://doi.org/10.1109/TPEL.2018.2834409.

[9] X. Wu, G. Tan, Z. Ye, Y. Liu, and S. Xu, 'Optimized common-mode voltage reduction PWM for three-phase voltage-source inverters', *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2959–2969, 2016, doi: https://doi.org/10.1109/TPEL.2015.2451673.

[10] J. Lee and J. W. Park, 'Selection of PWM Methods for Common-Mode Voltage and DC-Link Capacitor Current Reduction of Three-Phase VSI', *IEEE Trans. Ind. Appl.*, vol. 59, no. 1, pp. 1064–1076, 2023, doi: https://doi.org/10.1109/TIA.2022.3213632.

[11] M. Wei, S. Huang, G. Liang, W. Liao, X. Wu, and S. Huang, 'An Optimal PWM Method With Reduced Common-Mode Voltage and Current Ripple for Three-Phase Voltage-Source Inverter', *IEEE Trans. Transp. Electrif.*, vol. 11, no. 2, pp. 6799–6811, 2025, doi: https://doi.org/10.1109/TTE.2024.3516118.

[12] J. W. Kimball and M. Zawodniok, 'Reducing common-mode voltage in three-phase sine-triangle PWM with interleaved carriers', *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2229–2236, 2011, doi: https://doi.org/10.1109/TPEL.2010.2092791.