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A THREE-STAGE SEVEN-LEVEL CASCADED H-BRIDGE INVERTER WITH WIDE INPUT VOLTAGE RANGE FOR PV APPLICATIONS

Xuan-Bach Dang, Anh-Duc Vu, Trong-Nguyen Nguyen,
Manh-Hoan Nguyen*, Minh-Tan Tran

Faculty of Electrical Engineering Technology, Industrial University of Ho Chi Minh City, Ho Chi Minh City, Vietnam

*Email: *nguyenmanhhoan@iuh.edu.vn*

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ABSTRACT

The increasing demand for high efficiency power conversion systems with stringent power quality requirements has promoted the development of multilevel inverters. Compared to conventional inverter configurations, multi-stage inverters can produce output voltage waveforms with lower harmonic distortions and improved efficiency. This study proposes a single-phase seven-level CHB inverter in which each H-bridge module is integrated with an independent two-stage boost converter, enabling stable operation over a wide voltage range typical of photovoltaic (PV) and energy storage system (ESS) applications. A dual-loop PI-based control strategy is implemented in the boost stage to regulate the intermediate DC-link voltages and indirectly stabilize the AC output voltage in conjunction with level-shifted pulse-width modulation. Simulation results demonstrate that the proposed system maintains stable and symmetric seven-level output voltage under significant input voltage variations. The experimental results are directly compared with the simulation results to validate the accuracy of the designed model and to confirm the reliability of the suggested topology, these results clearly highlight the novelty and key advantages of the proposed structure in extending the operating voltage range compared to conventional multilevel inverter configurations that typically require high and relatively stable DC input sources.

Keywords: CHB multilevel inverter, Two-stage boost converter, Wide input voltage range, Phase Disposition Pulse Width Modulation.

1. INTRODUCTION

The large-scale deployment of photovoltaic technologies in modern electrical networks requires power electronic converters with higher efficiency and improved dynamic performance. In renewable energy and energy storage systems, inverters serve a key function by converting DC power into AC for supplying loads or grid connection. However, PV and ESS sources typically exhibit low and highly variable input voltages due to changes in irradiance, temperature and state of charge, which creates significant challenges in maintaining a stable AC output voltage.

Conventional two-level inverter structures, although simple, suffer from several inherent limitations, including high total harmonic distortion (THD), the requirement for bulky output filters, increased power losses and reduced efficiency as the power rating increases [1], [2]. Consequently, multilevel inverter (MLI) topologies have attracted significant attention due to their ability to generate stepped voltage stress on power switches and improved overall

efficiency [3]. The three main categories of MLIs include Neutral-Point-Clamped inverters (NPC) [4], Flying Capacitor inverters (FC) [5] and Cascaded H-Bridge inverters (CHB) [6]. Among these, the CHB topology stands out due to its modular structure, scalability in voltage and power, reduced voltage stress on each switch and its suitability for distributed energy sources such as photovoltaic (PV) applications and energy storage systems (ESS) [7], [8]. The proposed topology results in a higher component count and increased cost. However, it significantly improves power quality and enables stable operation over a wide input voltage range.

In conventional CHB configurations, each H-bridge module requires an independent DC source with high and stable voltage range, a DC-side boost converter is typically integrated; however, traditional boost converters require high duty cycles to achieve large voltage gains, which in turn triggers increased current ripple, higher losses and control stability issues [9]. Although high-gain topologies such as coupled-inductor and switched-capacitor converters offer higher voltage conversion ratios, they suffer from increased structural complexity and reduced reliability [10], [11].

Several advanced topologies, such as Z-source, quasi-Z-source, switched-boost, and quasi-switched-boost converters, have been proposed to integrate voltage boosting capability into the inverter [12]-[14]. However, these approaches still rely heavily on passive component networks, leading to increased complexity. However, maintaining stable DC-link and AC output voltages remains challenging when the input from PV and energy storage systems varies continuously. Furthermore, the transient response characteristics of the voltage regulation system deteriorate when the input source undergoes rapid variations over time. In contrast, the two-stage boost approach provides a more effective solution by offering higher voltage gain, improved controllability, and better adaptability to wide input voltage variations in PV/ESS systems [15].

Based on the previous analyses, a redesigned three-stage CHB inverter structure is developed to achieve wide-range input voltage operation while retaining structural simplicity and stable output voltage characteristics. To achieve this, each CHB module is independently integrated with a dedicated cascaded boost converter structure. This structure integrates the modular characteristics of the CHB inverter with the high voltage amplification capability of a dual-stage boost converter. As a result, the inverter can operate with low and wide-ranging input voltages (5-20V), while ensuring a stable DC-link voltage for each stage. The two-stage boost configuration also reduces the required voltage gain per stage, minimizes current ripple, decreases switching losses, and improves the stability of the PI controller PSIM simulation results demonstrate that with three cascaded modules, the proposed topology achieves an output voltage of 300 V with a smooth sinusoidal waveform, maintaining stable operation when the input voltage varies from 7V to 22V and load resistance changes between 200 Ω to 500 Ω. The harmonic distortion level is maintained below 3.7%, and the dynamic response is fast. The proposed structure significantly reduces the voltage load across the switching components.

The manuscript is structured as follows. The introduction of this research is provided in Section 1, whereas the proposed converter structure is discussed in Section 2. Section 3 presents the control method. Section 4 analyzes converter efficiency and power loss. Section 5 discusses simulation and experimental validation, while Section 6 summarizes the main conclusions.

2. PROPOSED THREE-STAGE SEVEN-LEVEL INVERTER TOPOLOGY

2.1. Proposed Cascaded H-Bridge Inverter Topology

Fig. 1 illustrates the proposed three-stage seven-level inverter integrated with a cascaded boost converter. The input stage employs an enhanced dual-stage boost converter to increase the supplied voltage level. The back-end stage is an H-bridge inverter comprising four power

switches to generate the output voltage Vo. Through the combined action of the boost unit and the H-bridge inverter, a seven-level waveform can be achieved.

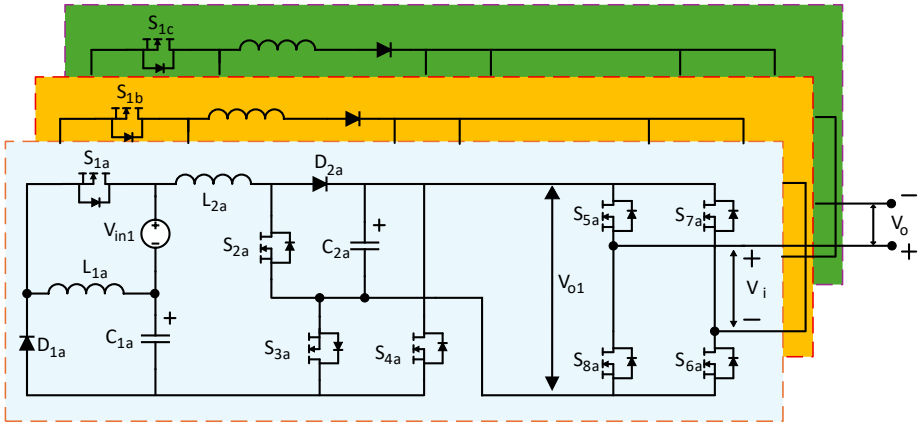


Fig. 1. Proposed three-stage seven-level inverter topology.

2.2. Operation principle of the Two-Stage Boost Converter

Assuming identical module parameters, module 1 is considered for operating mechanism analysis. The CCM operation of the cascaded Buck-Boost/Boost converter is examined, including switch states, inductor energy transfer, and stage voltage boosting based on Fig. 2.

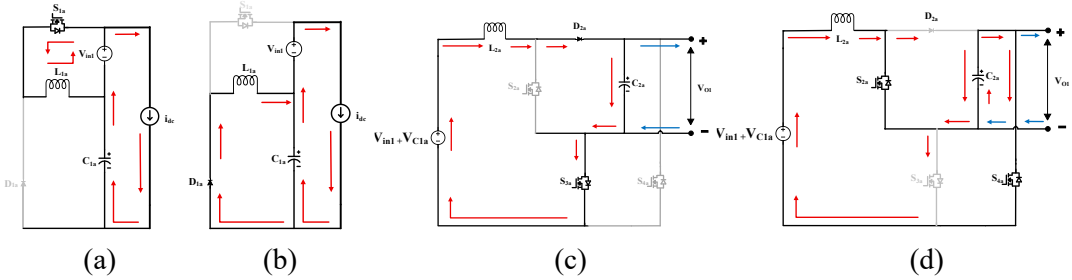


Fig. 2. Structure and operating states of the two-stage boost converter on the module 1: (a) Operating State I; (b) Operating State II; (c) Operating State III; (d) Operating State IV.

Operating modes of the circuit:

Mode I (S_{1a} ON)

In Mode I, S_{1a} conducts and the source current charges inductor L_{1a}, while diode D_{1a} remains reverse-biased. Hence, the inductor voltage is given by:

$$U_{L1a} = U_{S1a} = L_{1a}(di_{L1a}/dt) \quad (1)$$

where U_{L1a}, U_{S1a}, L_{1a}, and di_{L1a}/dt represent the inductor voltage, switch voltage, inductance value, and the rate of inductor current, respectively.

Therefore, the inductor current ripple during S_{1a} ON-state is:

$$(\Delta i_{L1a})_{closed} = D_1 T(V_{in1}/L_{1a}) \quad (2)$$

where Δi_{L1a}, V_{in1}, T, D_1 denote the current ripple, input voltage, switching period, and duty ratio, respectively.

Mode II (S_{1a} OFF)

In Mode II, when switch S_{1a} turns OFF, the stored inductor energy is transferred through diode D_{1a} to the capacitor and load. The inductor voltage then equals the capacitor voltage.

$$(\Delta i_{L1a}/\Delta t) = [\Delta i_{L1a}/(1 - D_1)T] = V_{C1a}/L_{1a} \quad (3)$$

From Equation (3), the inductor current ripple when switch S_{1a} is OFF is given by:

$$\Delta i_{L1a})_{open} = (1 - D_1)T(V_{C1a}/L_{1a}) \quad (4)$$

where V_{C1a} represents the voltage across capacitor C_{1a}

From Equations (2) and (4), it can be obtained that :

$$D_1T(V_{in1}/L_{1a}) - (1 - D_1)T(V_{C1a}/L_{1a}) = 0 \quad (5)$$

Based on Equation (5), by analyzing the operating state of the first-stage Buck-Boost converter, the relationship between the intermediate voltage V_{C1a} and the input voltage V_{in1} is derived as:

$$V_{C1a} = V_{in1}D_1/(1 - D_1) \quad (6)$$

Mode III (S_{2a}, S_{4a} ON and S_{3a} OFF)

In Mode III, the combined voltages $V_{in1} + V_{C1a}$ are applied through switches S_{2a} and S_{4a} to charge inductor L_{2a}, while capacitor C_{2a} discharges to support the output voltage V_{o1}. This interval corresponds to the energy storage phase of the boost stage, preparing for power transfer to the load in the subsequent switching period.

When switches S_{2a} and S_{4a} are ON, the voltage across the inductor during the interval D_2T (where D_2 is the duty cycle) is given by:

$$(V_{L2a})_{closed} = V_{in1} + V_{C1a} + V_{C2a} \quad (7)$$

where V_{C2a}, V_{L2a} denote the capacitor C_{2a} and inductor L_{2a} voltages, respectively.

Mode IV (S_{3a} ON and S_{2a}, S_{4a} OFF)

In Mode IV, after the input sources $V_{in1} + V_{C1a}$ are disconnected, inductor L_{2a} transfers energy through diode D_{2a} to capacitor C_{2a}, thereby regulating the output voltage V_{o1} and preparing the system for the next switching cycle.

When switch S_{3a} is ON and switches S_{2a} and S_{4a} are OFF, the inductor voltage during (1-D_2)T is expressed as:

$$(V_{L2a})_{open} = V_{in1} + V_{C1a} - V_{C2a} \quad (8)$$

Substituting (7) and (8) into the steady-state condition yields :

$$D_2(V_{L2a})_{closed} + (1 - D_2)(V_{L2a})_{open} = 0 \quad (9)$$

Where D_2 denotes the second-stage duty ratio.

From Equation (9), after algebraic manipulation, the relationship between the output voltage V_{o1}, the input voltage V_{in1}, and the intermediate voltage V_{c1a} in the second stage of the boost converter is obtained as:

$$V_{o1} = [V_{in1} + V_{C1a}/(1 - 2D_2)] \quad (10)$$

Where V_{o1} denotes the module output voltage.

From Equations (6) and (10), it is evident that the expressions clearly describe the overall relationship among the output voltage, the input voltage, and the two duty cycles of the two-stage boost converter. The first stage is governed by D_1, while the boost stage is controlled by

D_2. By appropriately adjusting both duty cycles D_1 and D_2, the desired output voltage level can be achieved from a low initial input voltage:

$$V_{o1} = V_{in1}/[(1 - D_1)(1 - 2D_2)] \quad (11)$$

where V_{C2a} represents the voltage across capacitor C_{2a}

2.3. Operating principle of the H-Bridge Inverter

In this section, the switching behavior of the H-bridge inverter is examined in order to explain the generation mechanism of the seven-level AC output waveform.

Table 1. Switching combinations for each output voltage level

S_{5a}	S_{6a}	S_{7a}	S_{8a}	S_{5b}	S_{6b}	S_{7b}	S_{8b}	S_{5c}	S_{6c}	S_{7c}	S_{8c}	Voltage Level
1	1	0	0	1	1	0	0	1	1	0	0	$+3V_i$
1	1	0	0	1	1	0	0	0	1	0	1	$+2V_i$
1	1	0	0	0	1	0	1	0	1	0	1	$+V_i$
0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	$-V_i$
0	0	1	1	0	0	1	1	0	1	0	1	$-2V_i$
0	0	1	1	0	0	1	1	0	0	1	1	$-3V_i$

Each H-bridge inverter stage in the three-stage configuration is capable of generating three output voltage levels, namely $\pm V_i$, 0, where V_i is the input voltage of each module. By connecting the H-bridge units in series, the output voltage is obtained by combining the voltages generated by each module. As a result, the converter is capable of producing seven discrete voltage steps, namely $\pm 3V_i$, $\pm 2V_i$, $\pm V_i$, 0 which are suitable for multilevel modulation schemes. The detailed semiconductor switching combinations corresponding to each voltage level are listed in Table I.

Based on this model the operational behavior of the single-phase inverter is analyzed. Under the assumption that no shoot-through condition occurs due to simultaneous switching within the same inverter leg, the inverter operation can be simplified into two main states: the zero-voltage state and the $\pm V_{dc}$ state. For clarity, only one H-bridge leg is considered, since all H-bridge modules have identical strutures and operating characteristics. The corresponding operating states are shown in Fig. 3.

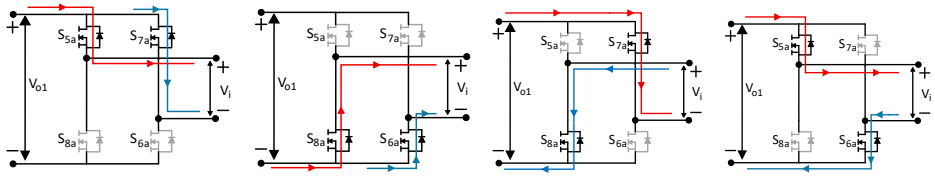


Fig. 3. Topology and switching states of the H-bridge stage on the module 1:
(a) State with S_{5a} and S_{7a} conducting; (b) State with S_{8a} and S_{6a} conducting;
(c) State with S_{7a} and S_{8a} conducting; (d) State with S_{5a} and S_{6a} conducting.

Based on the operating principles of the inverter switching components, the output voltage expressions are derived as follows:

Amplitude modulation index:

$$m_a = V_{ref} / V_{car} \quad (12)$$

where V_{ref} represents the magnitude of the sinusoidal reference waveform and V_{car} represents the amplitude of the carrier waveform.

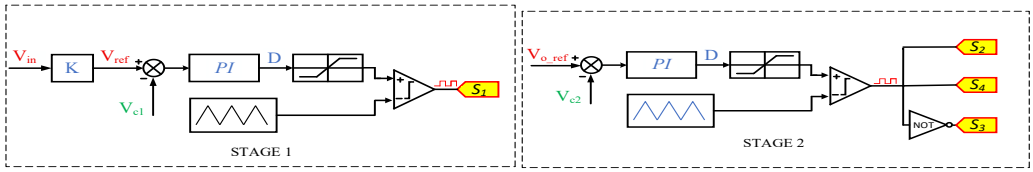
The output voltage generate by each H-bridge is given by:

$$V_i = m_a . V_{o1} \quad (13)$$

where V_i denotes the H-bridge output voltage of module 1 and V_{o1} the input voltage of a single H-bridge.

3. PROPOSED CONTROL STRATEGY FOR THE POWER CONVERTER

In the proposed configuration, the reference signal for the PWM generator is generated based on a PI (proportional-integral) control strategy, as shown in Fig. 4. The capacitor voltages C_1 and C_2 are actively balanced using a PI controller. Specifically, the circuit design allows the average charging and discharging currents to self-balance due to the symmetry of the switching states. The PI controller evaluates the error between the measured voltage and the reference value to regulate the switching duty cycle.



(a) (b)

Fig. 4. The structure of PI control for the two-stage boost module:
(a) Control of switch S_1 based on the input voltage feedback; (b) Control of switches S_2 and S_4 based on the output voltage feedback and switch S_3 uses the NOT signal.

The first control block, shown in Fig. 4(a), controls the operation of S_1 using a PI regulator to generate the PWM signal responsible for regulating the intermediate voltage between Stage 1 and Stage 2. This regulation ensures that the intermediate voltage is appropriately maintained to satisfy the output requirements under different load conditions.

The second control block, illustrated in Fig. 4(b), which controls switches S_2, S_3 and S_4, uses PI control to adjust the PWM signal for the boost stage

The selection of PI controller parameters is important for maintaining system stability, fast dynamic response, and minimized output error. In this study, the gains of the PI controllers, comprising the proportional constant K_p and the integral constant K_i, are calculated via the closed-loop Ziegler-Nichols experimental tuning method. To begin with, both K_p and K_i are set to zero. The K_p value is raised step-by-step until the critical gain K_u is reached, at which point the control loop output begins to exhibit sustained harmonic oscillations. The critical gain K_u, together with the corresponding oscillation period T_u, is used to calculate the PI controller parameters according to the Ziegler-Nichols tuning formulas:

$$K_p = 0.45K_u ; T_i = T_u / 1.2 \quad (14)$$

This method enables rapid identification of suitable control parameters, ensuring fast system response with a small steady-state error, and has been widely applied in industrial control systems. The use of a PI controller allows the system to achieve fast dynamic response and good stability, suppress output voltage oscillations, and adapts effectively to load variations. Consequently, the overall system performance is enhanced, and the output voltage is maintained with improved stability.

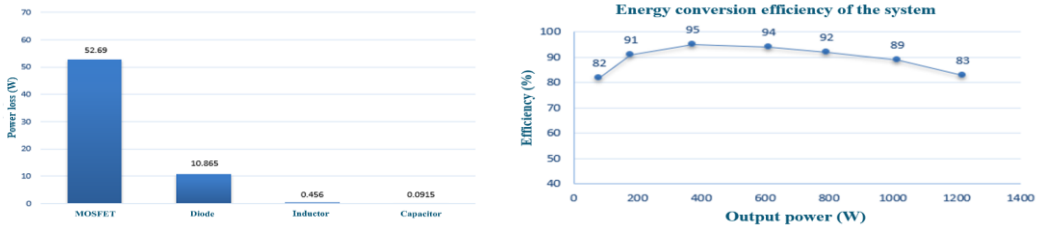
4. EFFICIENCY AND POWER LOSS ANALYSIS OF THE TWO-STAGE BOOST CONVERTER

To ensure that the simulation results are practically meaningful and accurately reflect the efficiency and power losses of the converter for evaluating the overall system performance, the component parameters in the numerical model are selected based on commonly used practical values. The main components include MOSFETs, diodes, inductors, and capacitors, whose detailed specifications are presented in Table 2.

Table 2. Component parameters

No.	Component	Parameter
1	MOSFETs	Model:STW45NM50;$V_{DS\_max} = 550$ V; $I_{D\_max} = 45$ A; $R_{DS\_on} = 0.08\Omega$; $T_{J_{max}}$=150 ℃
2	Diodes	Model:150EBU04;$V_{RRM\_max} = 400$ V; $I_{F\_max} = 150$ A; $T_{J_{max}}$=175 ℃
3	Inductors (L_{1a}, L_{1b}, *and* L_{1c})	Model:822797-SF; L = 300 µH; $I_{max} = 63$ A; DCR = 700 µΩ; Tolerance = 1%
4	Inductors (L_{2a}, L_{2b}, *and* L_{2c})	Model:1140-502K-RC; L = 500 µH; $I_{max} = 20$ A; DCR = 2.3 mΩ; Tolerance = 10%
5	Capacitors	Model:093 PMG-SI; C = 330 µF; $V_{max} = 420$ V; ESR = 0.43 mΩ; Tolerance = 20%

With the selected component parameters listed above, the simulation model was constructed using practical components. To assess the efficiency of the converter, the power losses in each major component were first analyzed. During the simulation, the power losses of the components (MOSFETs, diodes, inductors, and capacitors) were determined based on their electrical characteristics and the simulated current and voltage waveforms at each operating point.



(a) (b)

Fig. 5. (a) Power loss distribution among individual components;
(b) Efficiency characteristic of the two-stage boost converter with output power.

For semiconductor devices, including MOSFETs and diodes, PSIM calculates the losses by considering both conduction losses and switching losses, taking into account the dynamic and static characteristics of the devices. Regarding passive components (inductors and capacitors), the losses are mainly caused by the DC resistance associated with the inductors and the equivalent series resistance of the capacitors. These loss values are computed according to the RMS current flowing through the components during operation. The total power losses for each element are presented in Fig. 5.

Fig. 5(a) shows that the major power losses originate from the MOSFETs, followed by the diodes, while the losses in inductors and capacitors are negligible. Fig. 5(b) indicates that

the two-stage boost converter achieves high efficiency, peaking at medium output power and decreasing at higher power levels because of higher switching and conduction losses.

The overall power efficiency of the converter is calculated as follows:

$$\eta = (P_{out}/P_{out} + \sum P_{loss}) \times 100\% \quad (15)$$

Where P_{out} is the useful output power, and ΣP_{loss} is the total power loss, including the conduction and switching losses of the MOSFETs and diodes, the DCR losses of the inductors, and the ESR losses of the capacitors.

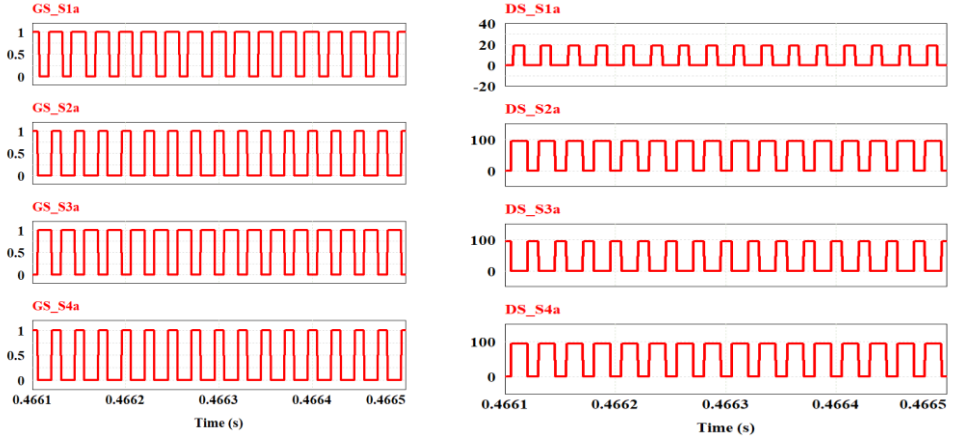
5. SIMULATION AND EXPERIMENTAL RESULTS

5.1. Simulation of the proposed structure

A detailed simulation model of the proposed seven-level inverter with a two-stage boost converter is developed using PSIM to evaluate its feasibility and performance, enabling stable operation over a broad input voltage range of 7 V to 22 V.

Table 3. Simulation parameters of the proposed inverter

Simulation parameter	Value
Supply voltages V_{in1}, V_{in2}, V_{in3} of the boost converters	7V-22V
Output voltages V_{o1}, V_{o2}, V_{o3}	100V
Carrier frequency of the boost converters	40 kHz
Capacitors C_{1j}, C_{2j} of boost converters (j denote a-c)	330 uF, 500 uF
Inductors L_{1j}, L_{2j} of boost converters (j denote a-c)	300 uH, 500 uH
Load resistance	200 Ω to 500 Ω



(a) (b)

Fig. 6. Operating states of the switches in the two-stage boost converter: (a) switching pulse waveforms of the switches; (b) voltage waveforms across the switches during operation.

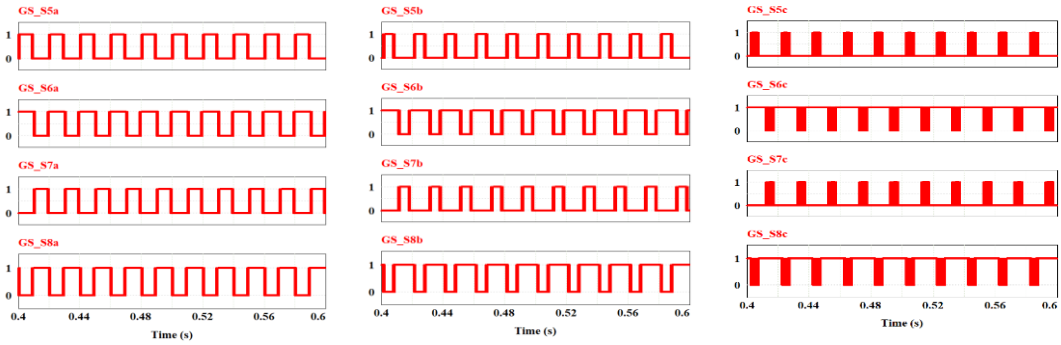


Fig. 7. Gate pulses of the switches in the cascaded H-bridge inverter: (a) H1; (b) H2; (c) H3.

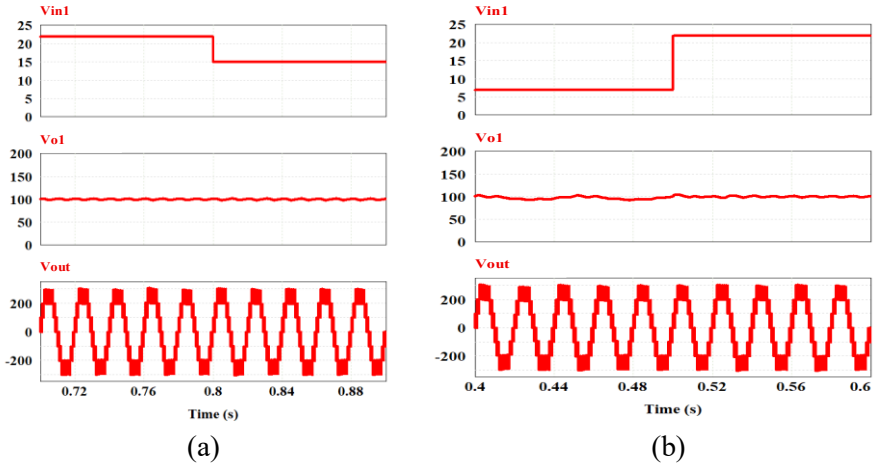


Fig. 8. Simulation results of the boost converter output voltage V_{o1} and the seven-level output Vout under input voltage variations V_{in}: (a) increase from 7 V to 22 V; (b) decrease from 22 V to 15V.

Fig. 8 illustrates the system response to input voltage variations from 7V to 22V and back to 15V. The output voltage V_{o1} is well regulated at 100V with symmetric voltage steps and no sustained oscillations, demonstrating the effectiveness of the PI controller under fluctuating input voltage conditions.

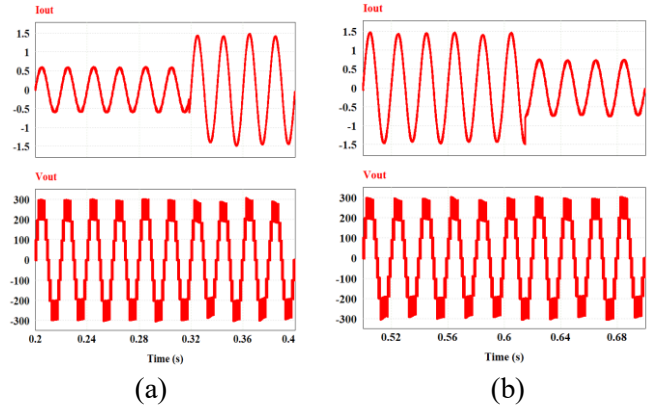


Fig. 9. Simulated waveforms of the output voltage Vo and load current Iout under different load conditions: (a) 500 Ω to 200 Ω; (b) 200 Ω to 400 Ω.

Fig. 9. illustrates the system response under load variations from 500 to 200 and from 200 to 400. The output voltage V_o is maintained at a peak value of 300V, demonstrating the effective regulation capability of the two-stage PI controller under varying load conditions.

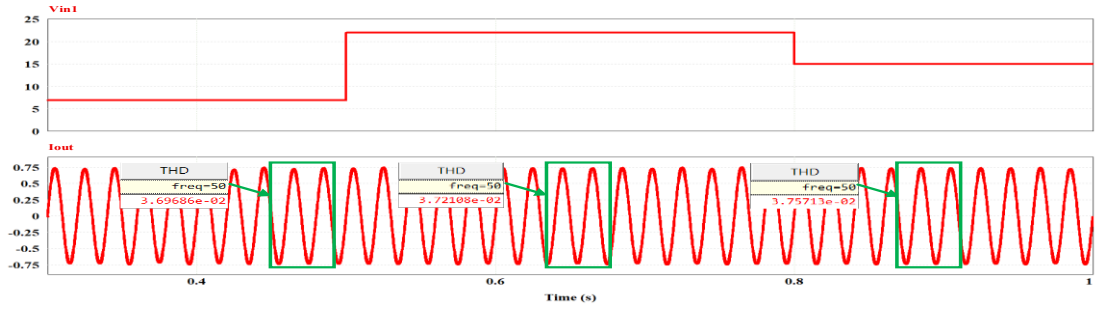


Fig. 10. Output current THD at 0.75A for different input voltages V_{in1} of 7 V, 22 V and 15 V

Fig. 10 illustrates the output current Iout under input voltage variations from 7 V to 22 V and back to 15 V. The current exhibits a near-sinusoidal waveform with low THD, demonstrating effective output current quality control under varying input voltage conditions.

5.2. Experimental results and evaluation

The experimental setup is constructed to validate the theoretical analysis and simulation results, as illustrated in the figures below.

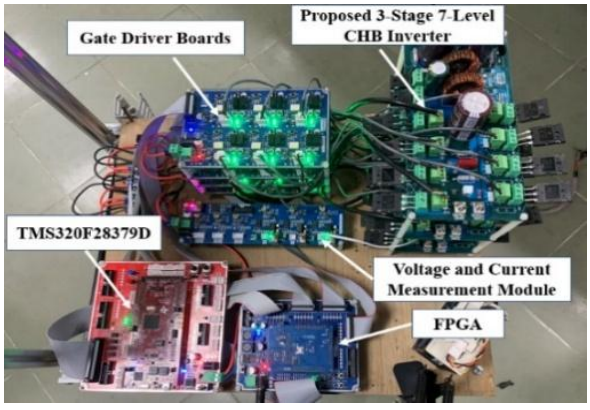
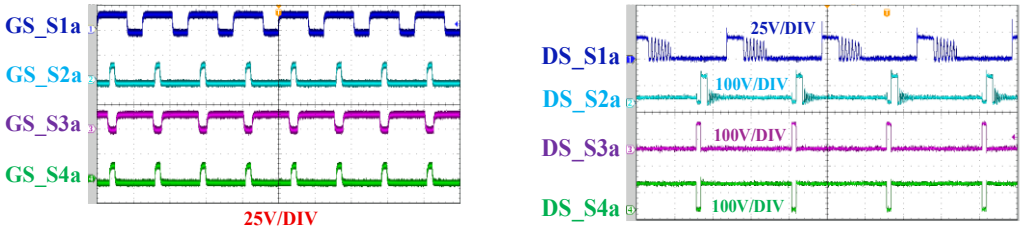


Fig. 11. Experimental setup of the proposed inverter.



(a) (b)

Fig. 12. Experimental results of the two-stage boost converter: (a) gating signals of the four controlled switches; (b) voltage waveforms across the corresponding switches.

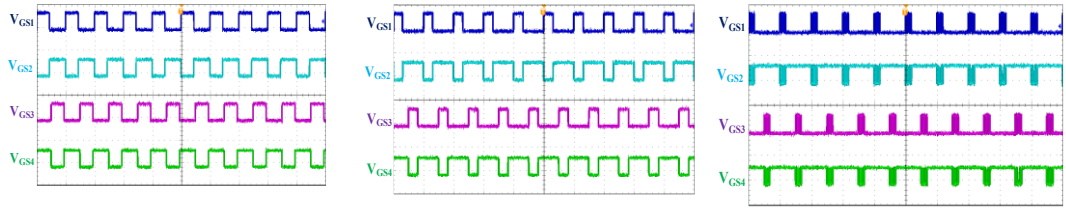


Fig. 13. Experimental gating signals of the switches in the three cascaded H-bridge inverter modules: (a) H1; (b) H2; (c) H3.

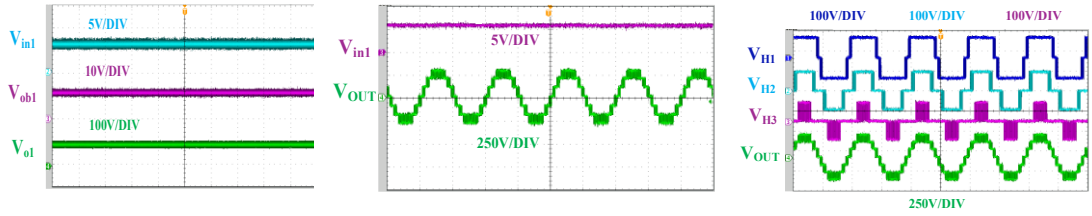


Fig. 14. Experimental voltage waveforms and control signals of the inverter: (a) input voltage and intermediate DC-link voltage of the module; (b) AC output voltage of a single H-bridge module; (c) voltages of H-bridge modules H1, H2, H3 and the overall output voltage Vout.

Based on Fig. 14, the fundamental operating principles of the three-stage seven-level inverter are experimentally verified, and the stable operation of the hardware prototype over a wide input voltage range enabled by the integrated boost converter is clearly demonstrated.

6. CONCLUSION

This paper proposes and successfully implements a cascaded seven-level inverter topology in which each module is combined with a two-level DC-DC boost conversion system, aiming to significantly enhance the input voltage operating capability and enable the use of low-voltage DC sources with wide voltage variations, as typically encountered in photovoltaic (PV) and energy storage system (ESS) applications. Unlike conventional multilevel inverter configurations that require relatively high and stable DC input sources, the proposed topology provides active voltage boosting capability, ensuring stable intermediate DC-link voltages for each inverter stage even under large input voltage variations. Hardware validation results demonstrate the ability of the system to generate well-defined output voltage levels in accordance with the operating principle of a seven-level multilevel inverter, while maintaining stable voltage waveforms over the entire investigated input voltage range. These outcomes highlight the effectiveness and main benefits of the proposed topology regarding wide input voltage operation, while preserving modularity, a reasonable component count and good output voltage quality. The preliminary experimental findings confirm the feasibility of the proposed system and serve as a basis for future investigations on voltage regulation, output filtering, and power quality evaluation.

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